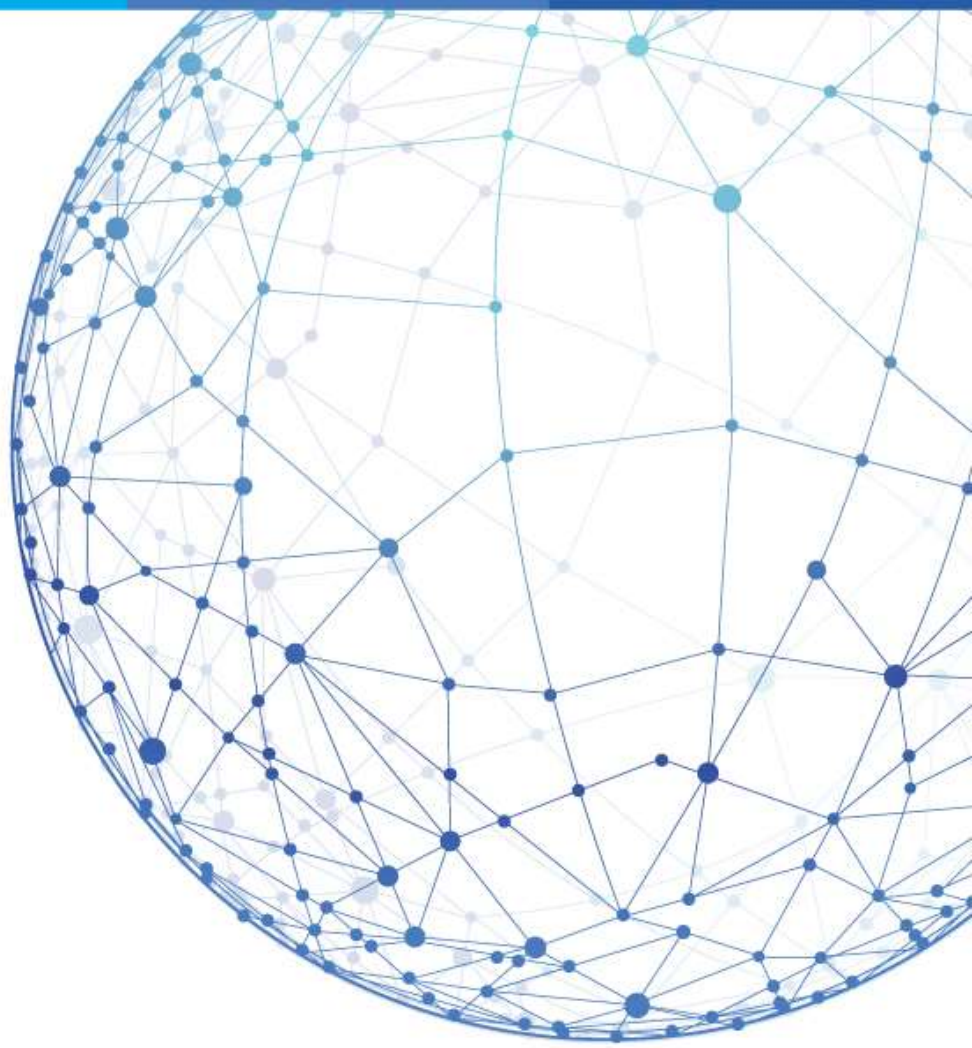
WHY DATE CODE RESTRICTIONS ARE OBSOLETE

THE DATA SUPPORTING SAFE LONG-TERM STORAGE



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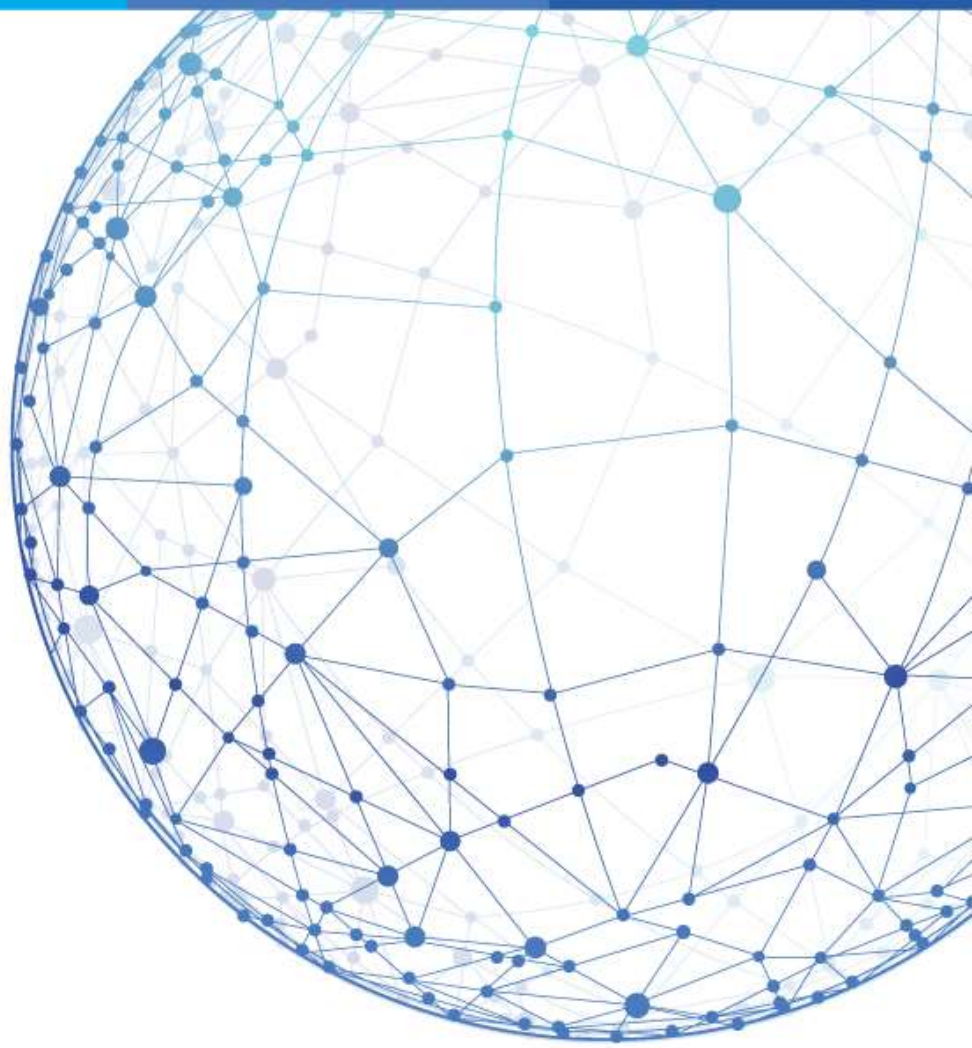
THANK YOU FOR JOINING US

Presenter: Dan Deisz,
Rochester Electronics Vice President, Design Technology

Email: ddeisz@rocelec.com



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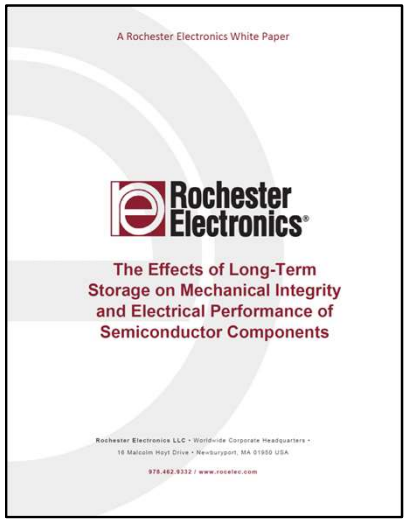
WHY DATE CODE RESTRICTIONS ARE OBSOLETE

This webinar is based on three papers published by Rochester Electronics on the topic of long-term storage (LTS) focusing on component solderability, mechanical integrity, and electrical test.



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Agenda

- **Trends in semiconductor manufacturing and lifecycles**
- **Options for extending component availability**
- **Overview of traditional solderability test methods per EIA/IPC/JEDEC J-STD-002**
- **Results of solderability studies on long-term stored devices**
- **Summary and Q&A**

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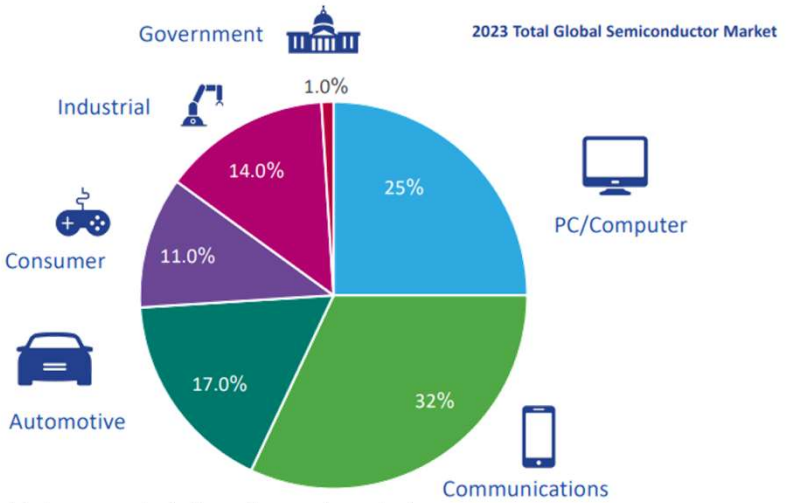
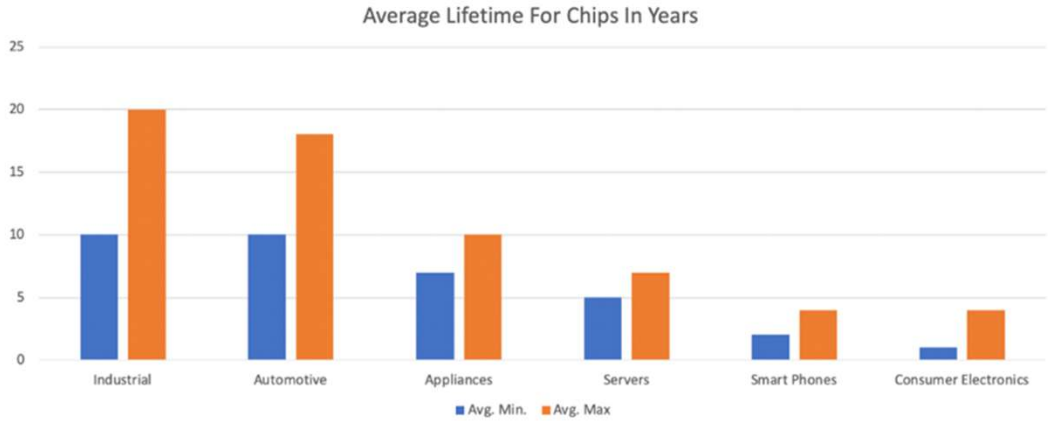
Industry Update - Markets



End-use market share for semiconductors
(Source: WSTS & SIA May 2024)

- 2024 = $626B, 2023 = $526.9B, 2022 = $574B
- Overall semiconductor revenue shrunk in 2023 by ~$50B while automotive grew by $9B.
- Chart is 2023, but segmentation is roughly the same

- Applications such as consumer, computing, and communications drive demand for semiconductors
- However, these applications have short lifetimes (Typically, <7 years)



Industry estimates on expected lifetimes of chips
Source: Industry estimates/Semiconductor Engineering

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Industry Update - Markets

- AI companies show most of the growth, but most others are flat with much slower growth.
- Fairly dramatic increase in spending forecasted for the 1% market, but not likely to change overall percentage or segmentation of the semiconductor market.

Source: Futurum Research, February 2025 & Worldwide Semiconductor Trade Statistics (WSTS)

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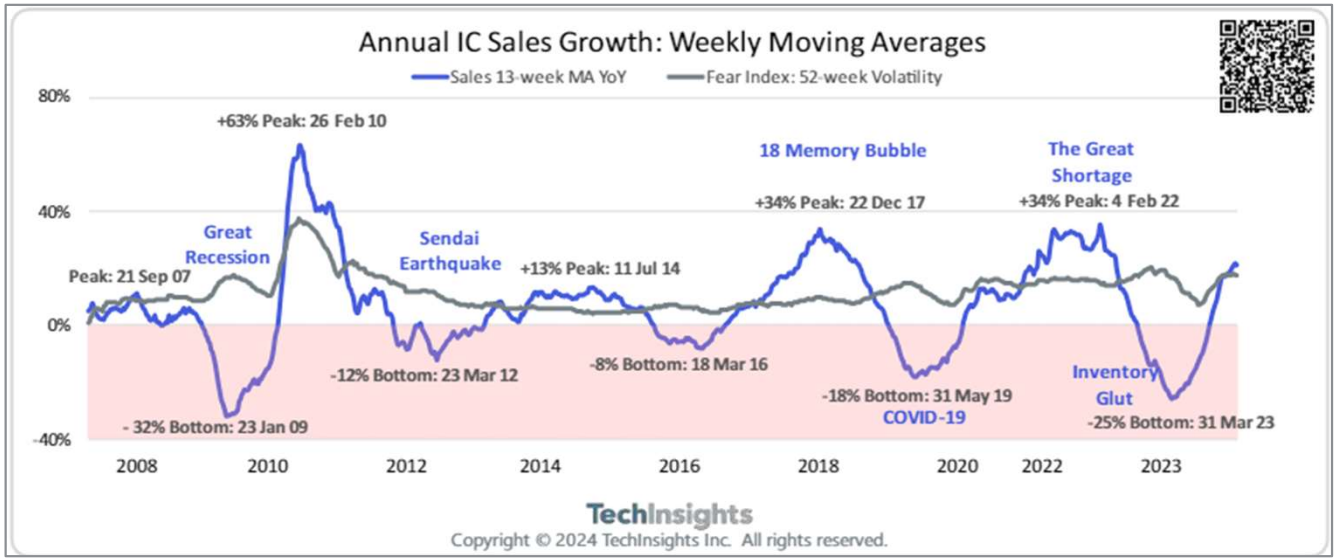
Industry Update Trends - Sales

- Semiconductor cycles are a fact of the industry
- The industry appears to be past the low in this cycle and is slowly trending back to growth
- Tough to predict in this geopolitical climate



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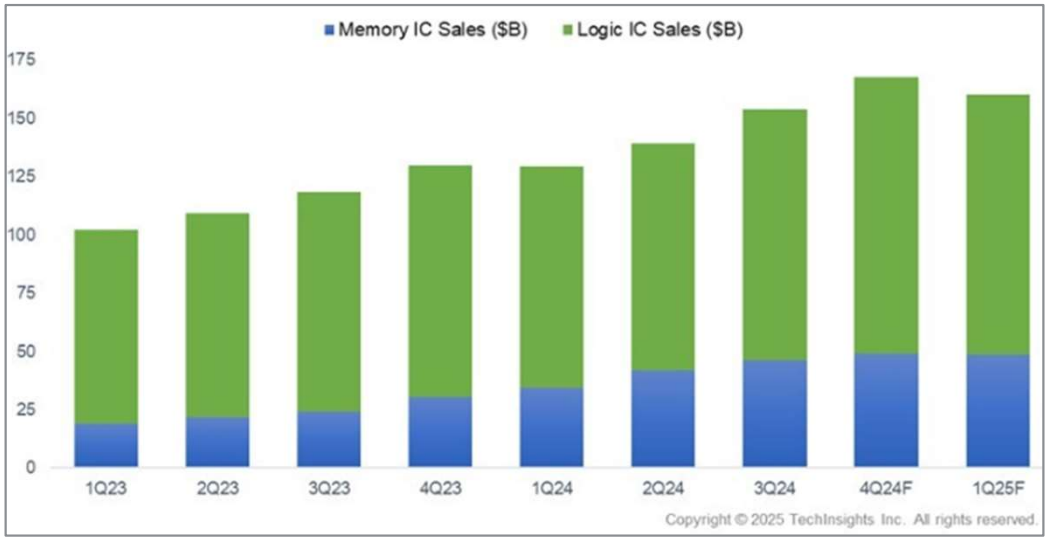
Industry Update Trends - Sales



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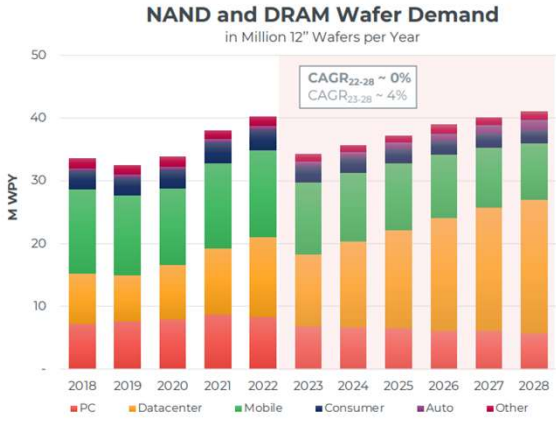
Industry Update Trends - Sales

- onsemi had a huge ASIC EOL event (LTB date was March 2024)
  - The last of the old-fashioned ASIC suppliers

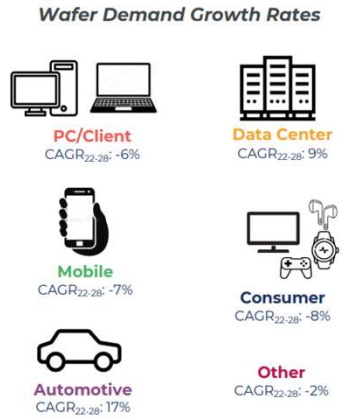
- The Chips Act investments were almost entirely in leading-edge silicon and assembly. Not sure about future investments.
  - The Chip Act grants are close to total **annual** R&D by TSMC of $30B

- PowerPC still exists in avionics…but the end is near.
  - Another massive EOL event at the end of 2023, NXP eliminated more than 30 PPC types.

- HBM (high bandwidth memory) drives wafer volume for memories, not stand-alone memory devices classically used in long-term systems. **Future issue?**



Source: DRAM and NAND market monitors (Q2-2023) by Yole Intelligence



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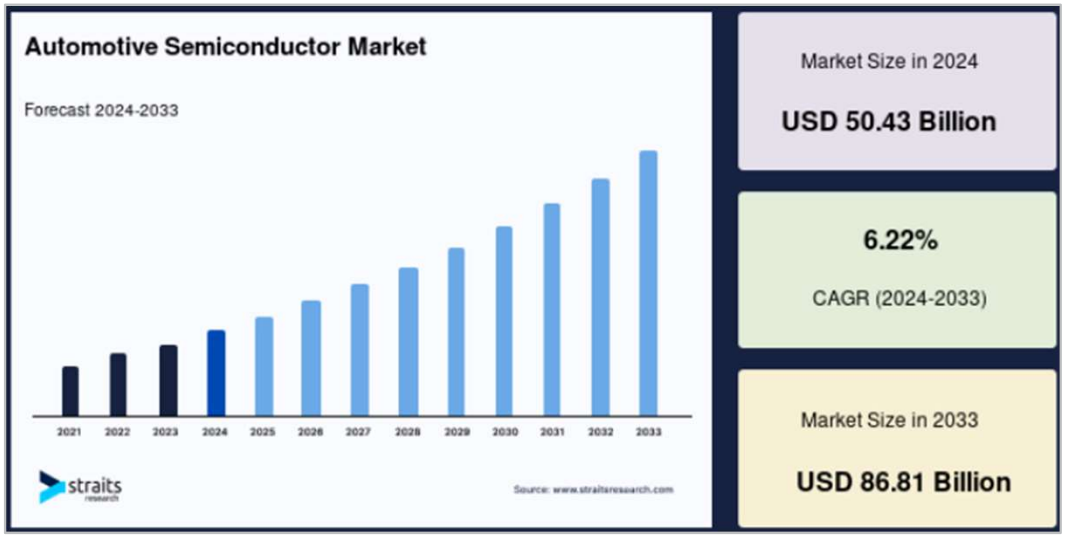
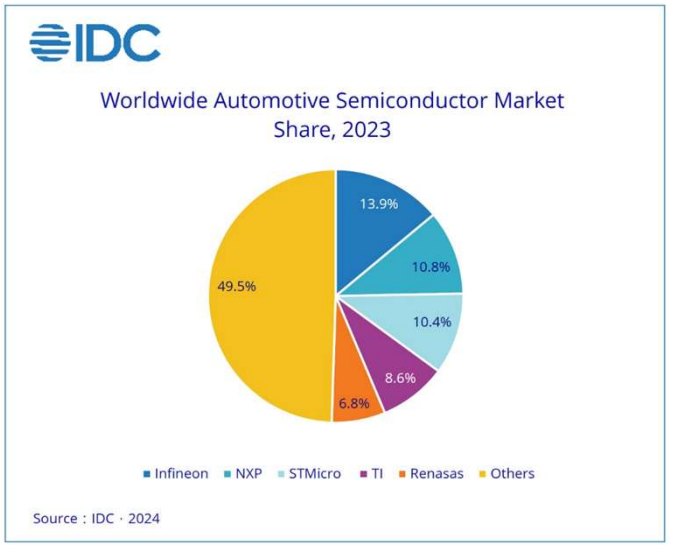
Industry Update Trends - Automotive

Automotive growth will result in more long-term storage of semiconductor products and continued demand to understand the quality of that stored product.





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Industry Update Trends: Commercial Avionics

- The commercial avionics backlog at Boeing and Airbus continues to be greater than 10 years.
- This will cause an extension of life for many systems coincident with lead frame packages that require trim-and-form tooling going away.
- Concerns about the quality of stored products will increase for this market segment.

Backlog

OEM Backlogs as of 28 Feb. 2025					
Airbus	A220	A320	A330	A350	TOTAL
	508	7,188	238	718	8,652
Boeing	737	767	777	787	TOTAL
	4,747	104	559	787	6,197

As of the end of February 2025, Airbus reported a backlog of 8,652 jets, of which 7,696—representing 89.0% of the total backlog—were A220 and A320 family narrowbodies. Airbus' all-time backlog record of 8,769 jets was set in October 2024. Meanwhile, Boeing's total unfilled orders (before ASC 606 adjustments) stood at 6,197 aircraft, with 4,735, or 76.4% of the total backlog being 737 MAXs. Boeing's highest recorded backlog of 6,268 aircraft was reached in November 2024. The volume of Airbus aircraft awaiting production and delivery represents 10.3 years of deliveries based on Forecast International's 2025 production numbers for Airbus. In comparison, Boeing's backlog would last approximately 10.9 years based on our 2025 production forecast.

February 2025 from Forecast International

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Industry Update Trends: Defense

- The worldwide defense markets are continually driving long-term demand with systems that get extended or that continue to be sold far beyond original forecasts
- Patriot, HIMARS, CH-53K Helicopter, and Eurofighter are examples
- Defense spending on a large upward trend

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Long-lifecycle supply chain risks and challenges

- **More components are becoming "obsolete" at a faster pace.**
  - Parts become obsolete when they are no longer manufactured by the original manufacturer (OCM)
- **Major OSATS moving:**
  - Away from lead frame assembly (DIPs, PLCCs, PQFP, etc.)
    - Those requiring trim and form tooling
  - To Pb-free options only
- **Suppliers consolidating product lines** – decreased production phase and increased EOL
  - Today's EOL/LTB brought on by a previously booming market and heightened product line focus
  - Seemingly endless supply chain challenges
- **Managing an OSAT supply chain is not real manufacturing**
- **The latest CHIPs Act investments are primarily for leading-edge technologies**
- **Strong growth in Fabless IC revenue – companies who do not dictate fab process availability**
  - Five of the top 10 semiconductor company revenue are fabless excluding foundries*

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Options for extending continuity of supply

1. **Last-time-buy and in-house long-term storage**
   - **Pros:** Ability to obtain the required number of components directly from the supplier
   - **Key issues:** Cash out, requires expertise and facilities, projections of long-term product needs, increase in component inventory

2. **Purchase of long-term stored components from an authorized distributor**
   - **Pros:** Ability to acquire components in a cost-effective manner
   - **Key issues:** Likely limited supply**,** Need to ensure components are new and unused (authorized suppliers only), concerns about quality/performance of aged components

3. **Work with a licensed manufacturer who is investing in their own manufacturing and is authorized to continue component supply**

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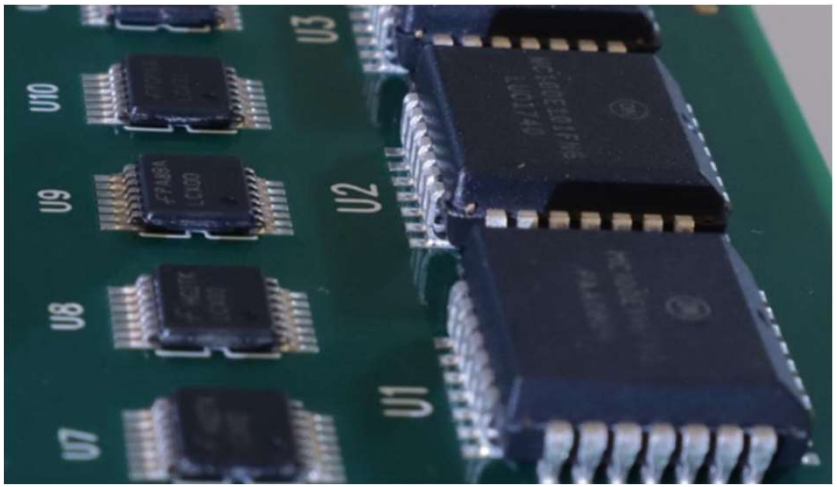
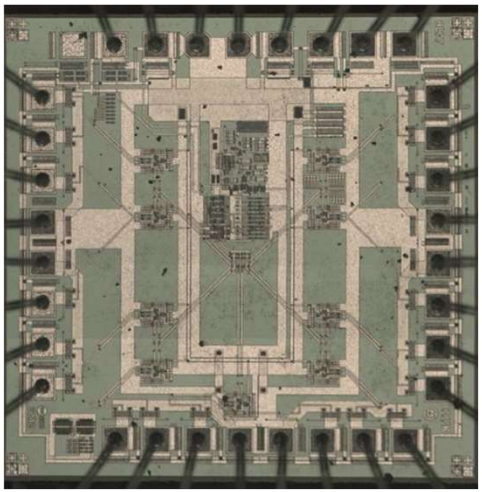
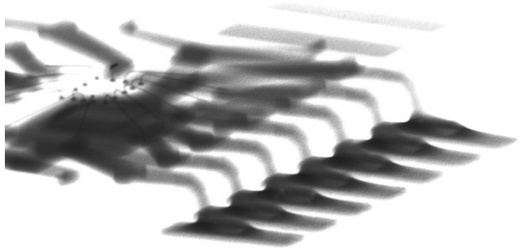
Previous studies of long-term storage

Package deconstruction & PCB assembly

- 57 devices per board
- Decapsulation & inspection
- Cross-sectioning & inspection







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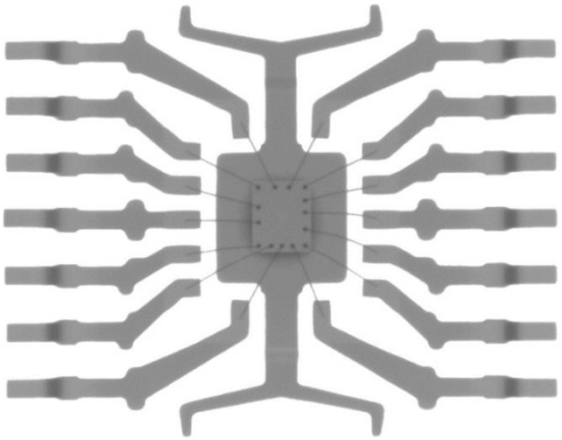
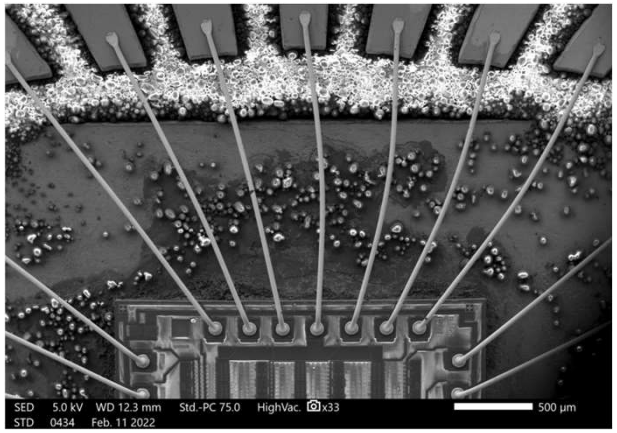
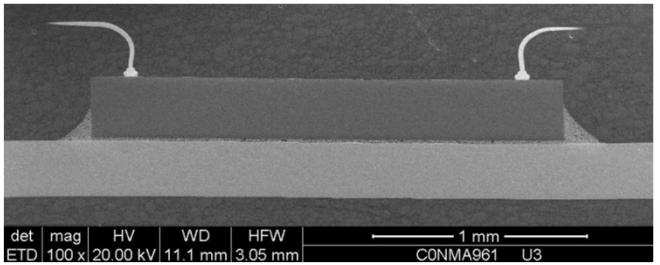
Previous studies of long-term storage

Package deconstruction & PCB assembly

- Devices 4 to 14 years in age
- Optical, X-ray, and SEM inspections
- No mechanical or electrical degradation







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EIA/IPC/JEDEC J-STD-002 Solderability Test Methods

Solder Bath / Dip and Look Test

- Robotic molten solder dip and inspection
- Analogous to wave solder board mounting
- **Pros:** Simple and widely available
- **Cons:** May not accurately reflect surface mount technology processing; incompatible with solder ball

Surface Mount Process Simulation Test

- Convection reflow of devices over printed solder paste pattern and inspection
- Analogous to SMT board mounting
- **Pros:** resemblance to end-use application
- **Cons:** test complexity and cost of reliable equipment

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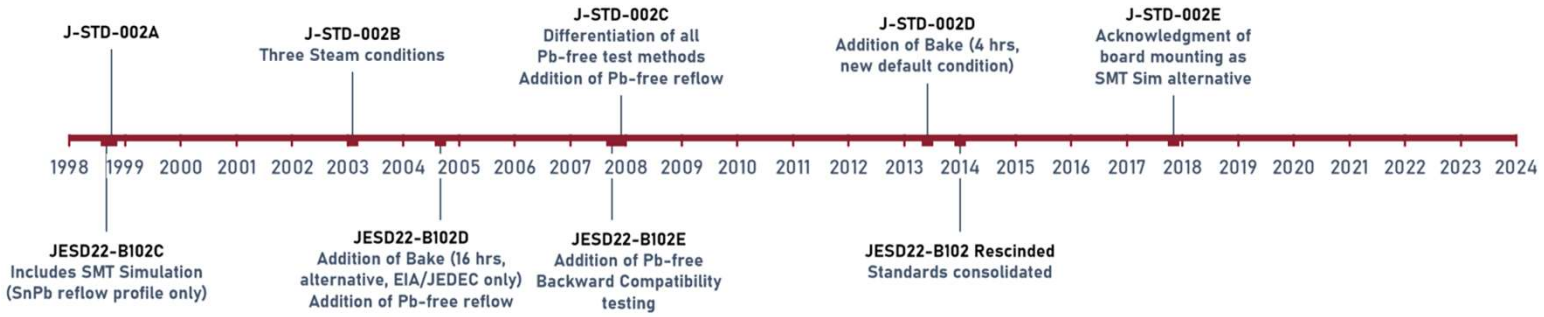
Industry Solderability Standard Evolution

Industry Standards for Solderability Testing

- Progressed to incorporate changes in technology
  - SnPb only to Pb-free, preconditioning methodology, etc.
- **Gradually shifted towards more resemblance of end-use process**
  - Dip and Look (long predates SMT Simulation)
  - Surface Mount Simulation (1999)
  - Physical Board Mounting (2017)

"*Actual demonstration of SMT in terms of **physical device mounting on printed boards** may be utilized as part of a solderability inspection operation that is performed as part of the documented assembly process **in lieu of SMT simulation**.*"

J-STD-002E § 4.2.9



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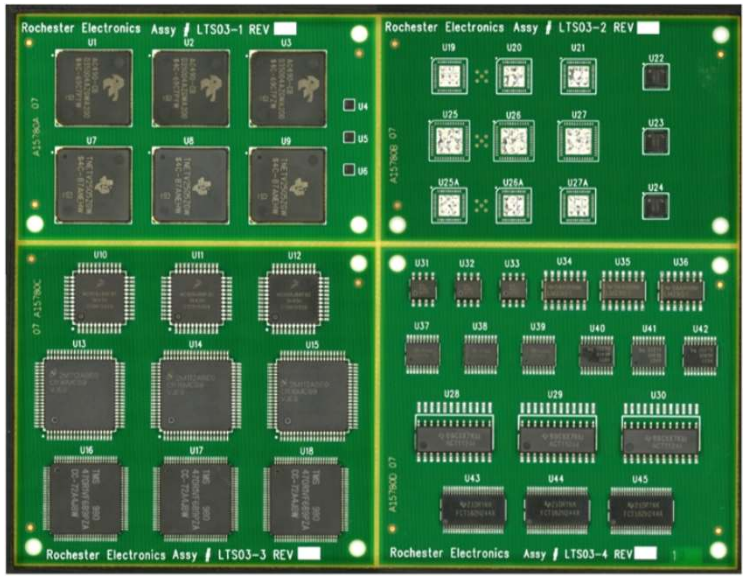
Study Design Philosophy



Component Focus

- Selected only **surface mount** devices
- Mix of package types: **SOIC, TSSOP, PQFP, QFN, BGA**
- Mix of termination types: **gull-wing, no-lead, solder ball**
- Mix of termination counts: from **8 to 240**
- Mix of device ages: from **8 to 22** years
    - Three distributed date codes per package type

Research Goals

- Determine solderability test methodology best suited for aged surface mount devices
- Enhance literature and industry understanding of date code relevance
- Benchmark Rochester Electronics capability for PCB attach testing against contract manufacturers

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Testing Methodology

Traditional Solderability Testing

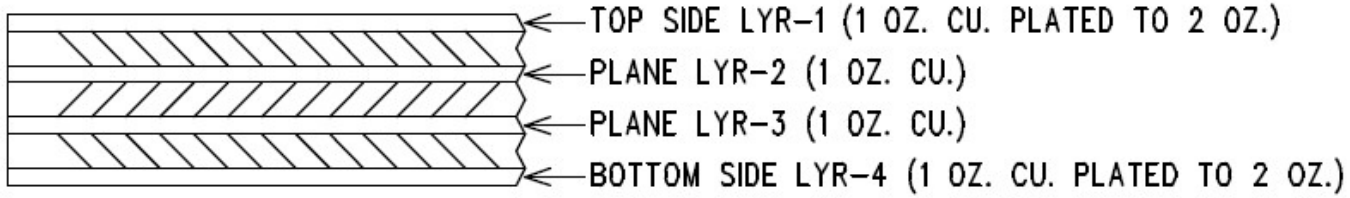
- Encompass J-STD-002 methods as practiced in industry
- Performed across three sites: **two independent testing providers** and **RE**
- Both preconditioning: **steam** and **bake**
  - **No pre-cleaning**, used **as-is**
- Both methods: **dip and look (A, A1, B, B1)** and **surface mount simulation (S, S1)**

Board Attach

- PCB designed to accommodate selected devices
  - **No pre-cleaning**, used **as-is**
- PCB assembled across four sites: **three independent contract manufacturers** and **RE**
  - RE using identical S1 reflow profile

Analysis

- Cross-sectioning and scanning electron microscopy of devices attached to boards



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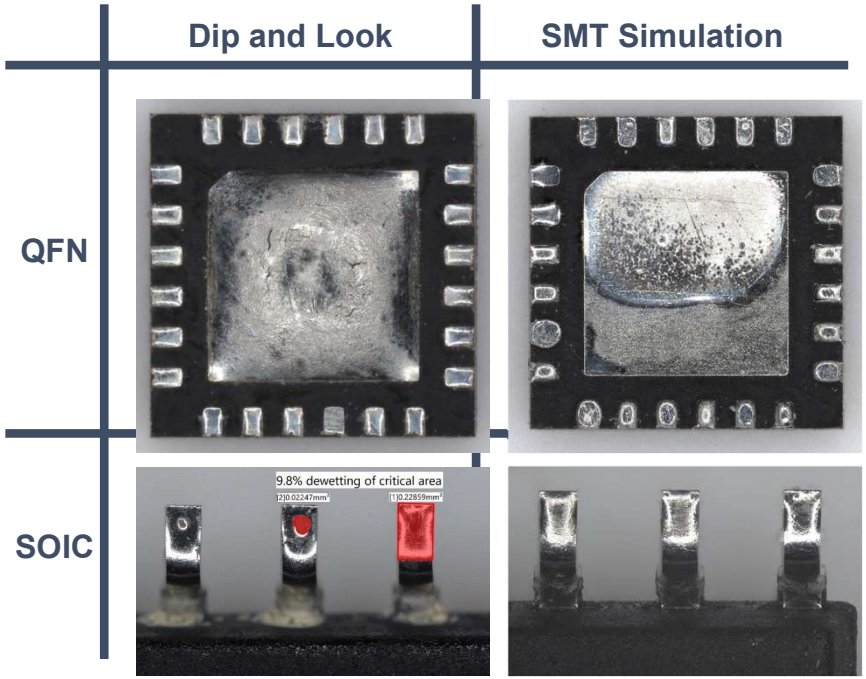
Traditional Solderability Method Comparison

Solderability Test Results

- Dip and look (J-STD-002 Test A1):
  - Good reproducibility
  - 29% of lots with observed defect
- SMT simulation (J-STD-002 Test S1):
  - Moderate reproducibility
  - 28% of lots with observed defect
- **Poor correlation** between the **dip and SMT** test methods

Overall Observations

- No correlation between failures and date code (device age)
- Some intra-lot part-to-part variation observed



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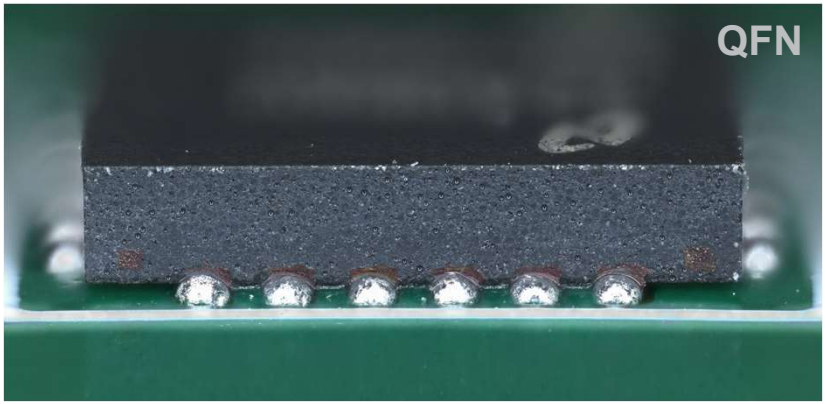
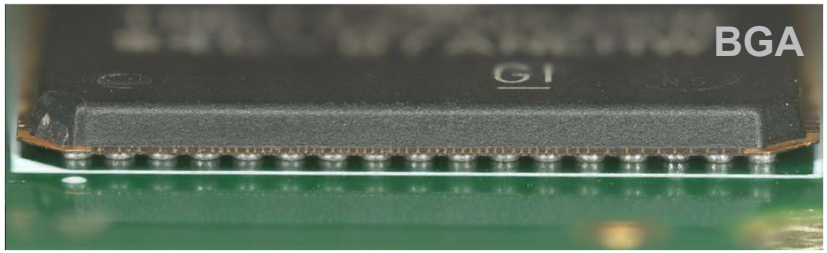
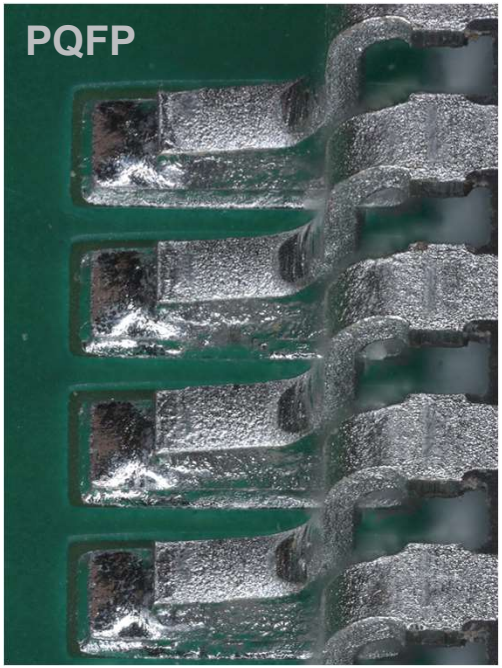
Assembled PCBs and Solder Joints







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Traditional Solderability Method Comparison

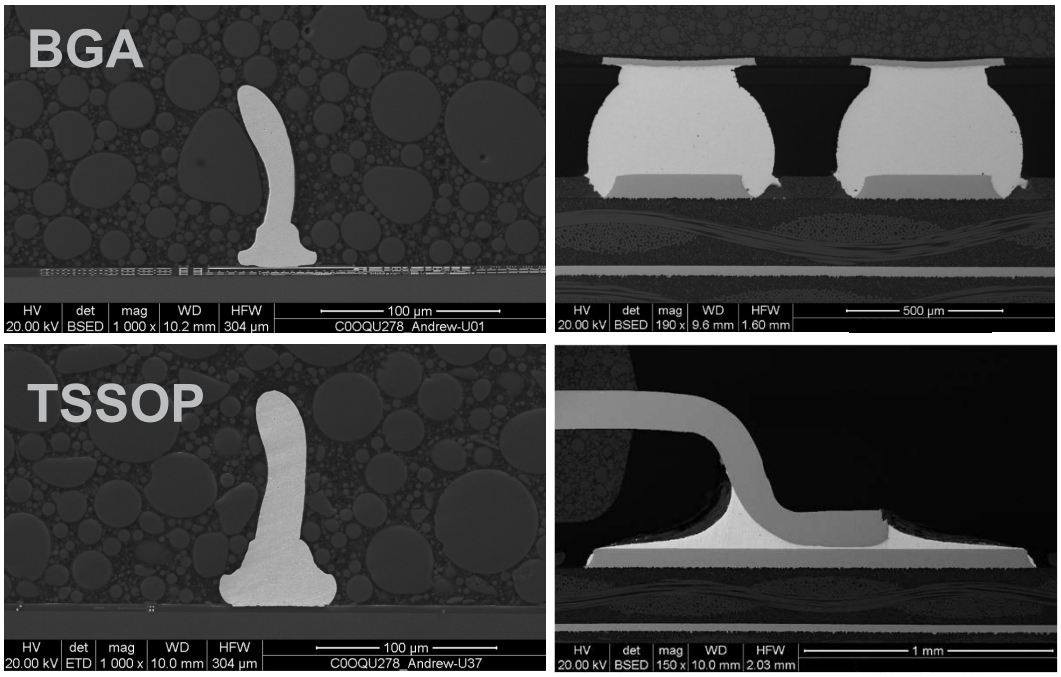
Cross-sectioned

- Solder joints
- Internal bond wires

SEM Imaged

- Scanning electron microscopy
- No nonwetting or delamination seen

No defects found



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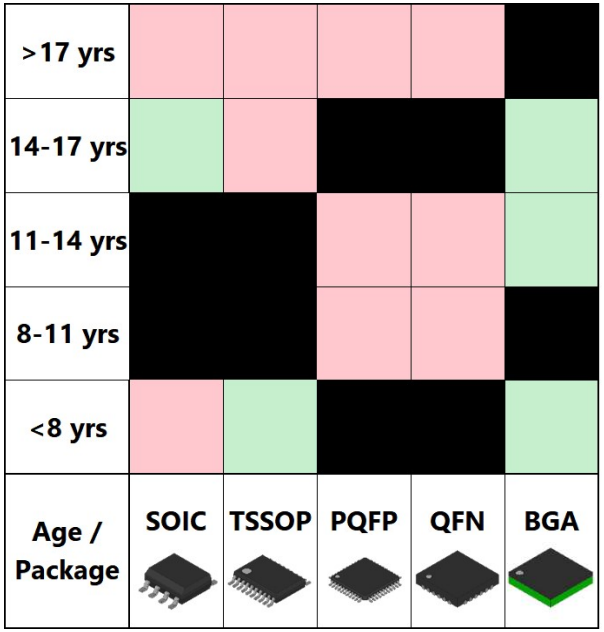
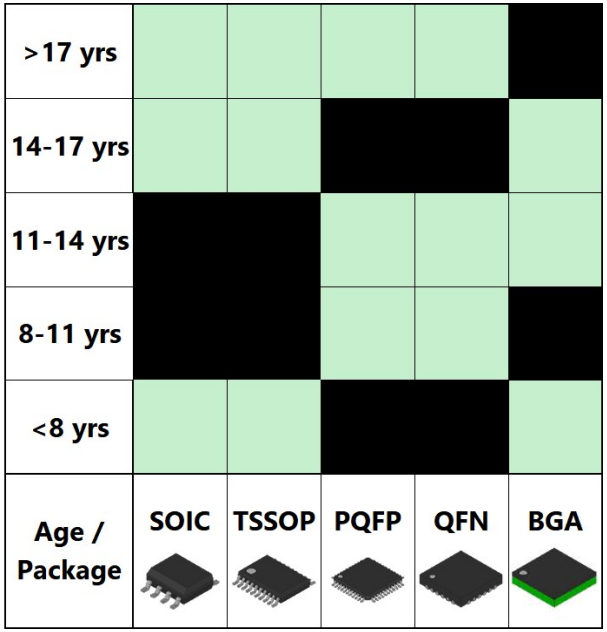
Results Overview

Traditional Solderability Testing



Board Attach



Reject found

No reject found

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Conclusions

- As lead frame assemblies that need trim and form go away, last-time manufacturing and storage will be a solution to ensure long-term availability
- In some cases, this will be the only way to avoid board redesign
- The industry must move away from unreasonable date code restrictions without technical basis and accept properly stored, fully authorized products.
- The data says that any date code restriction on Rochester Electronics products less than 15 years old has no technical merit—and Texas Instruments (among others) say the same thing about their stored products.
- Date code restrictions, such as 2-3 years from MFG dates, do not indicate the quality of components and may prevent perfectly usable components from being utilized.
- Given that most date code restrictions come from contract manufacturers, perhaps there is another reason for them.
- Keeps contract manufacturers from having to stock products, which would be very challenging
- System OEMs who use contract manufacturers should be pushing CMs away from date code restrictions on properly stored, fully authorized product

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Conclusions

- Purchasing from **Authorized distributors (AS6496A)** is an effective option to mitigate against unknown handling and storage found outside the authorized channel

- Rochester Electronics has conducted a detailed analysis of solderability, mechanical integrity, and electrical performance for components stored for **up to 22 years – No issues or failures were detected when properly stored.**
  - Multiple OCMs have conducted detailed analyses of components stored under controlled environments and concluded that **components can be used for >21 years**

- Using IPC/JEDEC J-STD-002 in the traditional way to judge solderability was found to be too restrictive
  - **Recommend J-STD-002E § 4.2.9 in lieu of SMT simulation**

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Questions?