# ECIA/JEDEC Experimentation on Solderability Test Preconditioning

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# ECIA/JEDEC Experimentation on Solderability Test Preconditioning

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## Abstract

This paper documents a series of three round-robin experiments hosted by the Association Connecting Electronics Industries (IPC) and the Electronic Components Industry Association (ECIA). The purpose of these experiments was to explore a suitable alternative for the steam preconditioning step that is included in the Component Solderability Test Standard, EIA/IPC/JEDEC J-STD-002 (herein after referred to as J-STD-002). It has been widely reported that the newer finishes performed very poorly in this high moisture environment. The first experiment describes the results of many different surface finishes on a range of different samples, which were subjected to one of many different pre-conditioning methods and then evaluated using a range of solderability test parameters. The second experiment was a confirmation run, repeating the results from the most promising pre-conditioning methods on a representative set of samples. The third experiment was an additional confirmation run, with a further exploration of the exact influence of solder temperature on solderability test results.

## Solderability Testing and Conditioning Methodology

The J-STD-002 specification utilizes several preconditioning methodologies for the purpose of assessing the quality of a solderable coating. The degradation of a component surface finish can be characterized by two primary mechanisms: (1) oxidation of the surface finish or the underlying base metal; (2) formation of an intermetallic compound (IMC) which diffuses through the surface finish and becomes oxidized. These two solderability degradation mechanisms occur at various rates dependent on the environmental conditions (e.g., temperature, humidity, air quality, etc.) and the initial quality of the component surface finish. The degradation of a component surface finish over time due to environmental exposure is termed “natural aging”. In order to have consistent, repeatable test practices across the electronics industry, the J-STD-002 specification has adopted “preconditioning” methodologies. Preconditioning is the term for the application of a specific set of temperature/humidity parameters for the purpose of degrading a component surface finish in a uniform, repeatable manner. Preconditioning methods are designed to cause the two solderability degradation mechanisms observed in natural aging but, because preconditioning creates accelerated reactions, it does not produce the same exact physical state as natural aging. The preconditioning methodologies utilized by the J-STD-002 specification have been characterized, tested and selected by the J-STD-002 specification committees as consistent and repeatable methods for stressing a component surface finish in a uniform way for the purpose of evaluating component surface finish quality.

## Introduction

In the 2009 to 2013 timeframe, a series of round robin experiments were conducted by members of the IPC Solderability Task Group and the ECIA Soldering Technology Committee. These experiments were conducted to evaluate an alternative to the steam preconditioning step that is included in the Component Solderability Test Standard J-STD-002. The committee members felt these experiments were necessary because in recent years a wider variety of surface finishes have become available for both components and circuit boards. Many companies had reported that the newer finishes perform very poorly after exposure to the high moisture content used in the steam preconditioning step, but that this degradation is unique to this conditioning, and does not occur during normal aging or during normal production. The committees agreed that an alternative was needed for the steam pre-conditioning step in the J-STD-002 solderability test.

The goal of this series of experiments was to find an alternative preconditioning environment that would be easy to specify, easy to maintain, and would allow the tester to identify components with finishes which would not be solderable in most assembly situations. Three experiments were conducted in all.

## Experiment 1 – Exploring Alternative Preconditioning Methods

The purpose of Experiment 1 was to evaluate an alternative conditioning methodology that was more applicable to finishes encountered today. There were two main goals of this experiment:

- Evaluate the effect of dry aging on component solderability performance.
- Assemble the data needed to make an informed decision on a suitable alternative conditioning environment.

Several candidate preconditioning methods were to be considered in this experiment. These candidates included:

- Dry bake 4 hours at 155°C (D04)
- Dry bake 8 hours at 155°C (D08)
- Dry bake 16 hours at 155°C (D16)
- Condition at 72◦C, 85 %RH for 8 hours (W08)

    - Note: This is the conditioning method for IPC-J-STD-003C: Solderability Tests for Printed Boards PWBs and is representative of a high temperature, high humidity conditioning method.
- As-received (AR) condition as a control.

Two test methods were used in Experiment 1 to evaluate the surface finish of the components:

- The Dip and Look test in J-STD-002, Test Method A1 and B1.
- The Wetting Balance test in J-STD-002 Test Method E1 and F1.

The test parameters used in Experiment 1 are shown in Table 1.

*Table 1 – Test Parameters used in Experiment 1*

| Step | | Dip and Look Test | Wetting Balance Test |
|---|---|---|---|
| Preconditioning | | Varied by Test Group | Varied by Test Group |
| Flux | Type | Activated Rosin (flux #2) | Activated Rosin (flux #2) |
| | Immersion Time | 5 – 10 sec. | 5 – 10 sec. |
| Solder | Type | SAC305 | SAC305 |
| | Temperature | 255ºC ± 5ºC | 255ºC ± 5ºC |
| | Immersion Time | 5 +0/-0.5 sec | 5 +0/-0.5 sec |
| Test Response | | % Dewetting | Time to Zero Force (sec)<br>Time to 2/3 Max Force<br>Force at 1 second<br>Max Force |

As shown in Table 2, thirteen different component sample configurations were used in Experiment 1.

*Table 2 – Component samples used in Experiment 1*

| Group | Base | Finish | Pin | Pkg | Supplier Pkg Descriptor |
|---|---|---|---|---|---|
| 1 | Cu | SnPb | 20 | SOIC | DW |
| 2 | Cu | NiPdAu | 20 | SOIC | DW |
| 3 | Cu | Sn | 20 | SOIC | DW |
| 4 | Cu | SnPb | 20 | PDIP | N |
| 5 | Cu | NiPdAu | 20 | PDIP | N |
| 6 | Cu | Sn | 20 | PDIP | N |
| 7 | Cu, Ni flash | SnPb | | Molded Cap | 7343 Molded Capacitor |
| 8 | Cu, Ni flash | Sn | | Molded Cap | 7343 Molded Capacitor |
| 9 | Cu | SnPb | 16 | DIP | Resistor Network |
| 10 | Cu | SnAgCu | 16 | DIP | Resistor Network |
| 11 | Cu dipped Ni Barrier | SnPb | | MLCC | 0805 MLCC |
| 12 | Cu dipped Ni Barrier | Sn | | MLCC | 0805 MLCC |
| 13 | Cu plated steel | SnBi | | V-Chip | 10mm V-Chip aluminum electrolytic |

These components include four different lead frame materials and five different lead finish materials. In all, there were 13 different test groups.

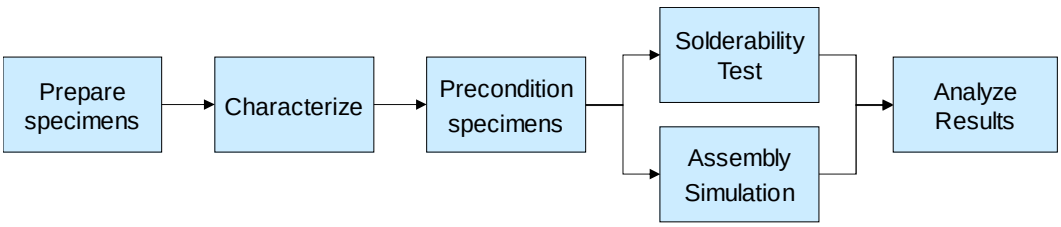
There were a range of response variables to be measured on each of the components.

- Dip and Look – Estimate percent coverage
- Wetting Balance – F@1 sec, Max force, Time to zero force, Time to 2/3 Max force
- Assembly simulation – percent acceptable solder joints
- Surface species analysis/Cross-section analysis
- Controls – as received

These steps were used to conduct the experiment and are shown in Figure 1.

1. Obtain the component samples (1000 each minimum)
2. Characterize as-received components
3. Prepare specimens
    a. Retain extra samples for later analysis
4. Perform preconditioning
    a. Divide into kits
    b. Send out kits
5. Design or obtain a test board
6. Perform solderability test with SAC305 (a lead-free alloy that contains tin, silver, and copper)
    a. Wetting balance
    b. Dip and Look
7. Perform assembly simulation
8. Analyze results

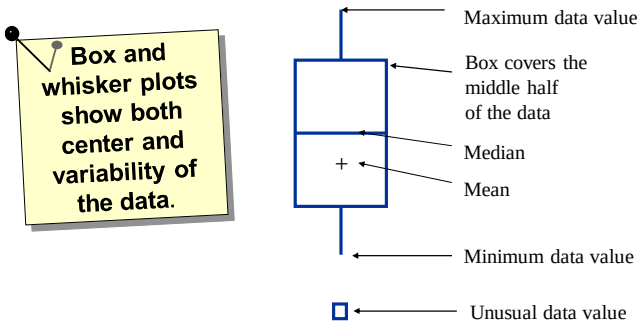
*Figure 1 – Steps used in Experiment 1*




There were three different statistical analysis methods used to analyze the data from Experiment 1.

**Analysis of Variance** - Used on the Wetting Balance data, where numerical measurements of performance were available. This method assessed whether or not the different conditioning methods influenced the measured solderability parameters. To visually depict these measurements, box and whisker plots were employed. Box and whisker plots used a special graphical icon explained in Figure 2.

*Figure 2 – Understanding Box and Whisker Plots*




**"Variance Components"** - The analysis of variance table divides total variance of a solderability parameter into components, one for each factor in the model. The effect of each factor is nested in the one above. The goal of such an analysis is to estimate the amount of variability contributed by each of the factors, called the variance components.

**Regression** - A technique for determining the mathematical relation between a measured quantity and the variables it depends on.

Experiment 1 – Summary Results

- No preconditioning method dominated the observed results.
  - This is a good result, reflecting on the number of component types and finishes in the DOE.
- Looking at the overall trends at a macro level, the results are reasonable.
  - As-received components performed better than preconditioned components.
  - Tin component finishes degraded more than tin/lead component finishes.
  - SAC component finish degraded more than tin/lead component finishes.
- Preconditioning for 4 and 8 hours at 155◦C were the better discriminators than the other preconditioning options.

Experiment 1 – Detailed observations

As Figure 3 showed, outliers were present in most graphs and formed a backdrop to almost all the analyses. Unexplained variation remained the dominant factor in each of the analyses. The unusual results may be attributable to statistical "noise" of the analysis that could obscure the ability to detect the "signal" that was the effect of the different preconditioning methods.

*Figure 3 – Box and Whisker plots illustrating the high number of outliers in the Experiment 1 data*

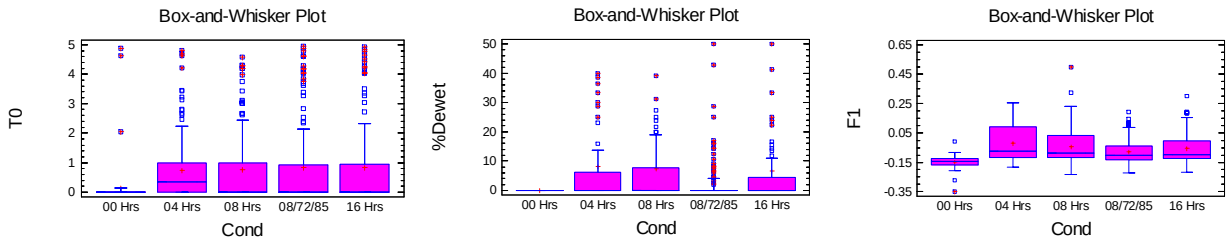



Table 3 shows a summary of the ANOVA data from Experiment 1. Red boxes show the conditioning methods which resulted in statistically distinguishable test results. Yellow boxes show the conditioning methods have marginally distinguishable test results. No Color, or blue boxes, show situations where the different preconditioning methods yielded similar results. The numbers in the boxes are the p-values of the ANOVA F-test, which shows the probability that the test results could occur if random chance were the only active agent. A p-value of 0.2045 would be 20.45%. A p-value of 0.05 or 5% was used as the significance level; 0.10 or 10% was used as marginally significant.

*Table 3 – ANOVA Results from Experiment 1*

| | | | | | | P-Value of AVOVA Test | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Group | Base | Finish | Pin | Pkg | Supplier Pkg Descriptor | T-2/3 | T0 | F1 | Fmax | %Dewet |
| 1 | Cu | SnPb | 20 | SOIC | DW | 0.0000 | 0.0002 | 0.0000 | 0.0000 | 0.0057 |
| 2 | Cu | NiPdAu | 20 | SOIC | DW | 0.0160 | NA | 0.0005 | 0.0486 | NA |
| 3 | Cu | Sn | 20 | SOIC | DW | 0.2045 | 0.0000 | 0.6468 | 0.0000 | 0.0000 |
| 4 | Cu | SnPb | 20 | PDIP | N | | | | | |
| 5 | Cu | NiPdAu | 20 | PDIP | N | | | | | |
| 6 | Cu | Sn | 20 | PDIP | N | | | | | |
| 7 | Cu, Ni flash | SnPb | | Molded Cap | 7343 Molded Capacitor | | | | | |
| 8 | Cu, Ni flash | Sn | | Molded Cap | 7343 Molded Capacitor | | | | | |
| 9 | Cu | SnPb | 16 | DIP | Resistor Network | 0.0139 | 0.3298 | 0.0137 | 0.0002 | 0.5350 |
| 10 | Cu | SnAgCu | 16 | DIP | Resistor Network | 0.0060 | 0.0090 | 0.5253 | 0.1931 | 0.6559 |
| 11 | Cu dipped Ni Barrier | SnPb | | MLCC | 0805 MLCC | 0.9457 | 0.9130 | 0.1399 | 0.0483 | 0.2012 |
| 12 | Cu dipped Ni Barrier | Sn | | MLCC | 0805 MLCC | 0.8490 | 0.8803 | 0.0558 | 0.0010 | 0.3095 |
| 13 | Cu plated steel | SnBi | | V-Chip | 10mm V-Chip aluminum electrolytic | 0.1393 | 0.4290 | 0.6610 | 0.8563 | 0.7018 |

The graphs in figures 4 through 6 below show results by package styles. The graphs show the averages, the bars show the 95 percent confidence limits on the averages.

*Figure 4 – Experiment 1 test results for Groups 1 to 3, the SOIC packages - (Top Yellow Boxes show ANOVA p-values, the bottom red X's and connecting lines illustrate which averages are close enough to be considered "not significantly different" in these results.) Graph shows average and 95% confidence interval.*

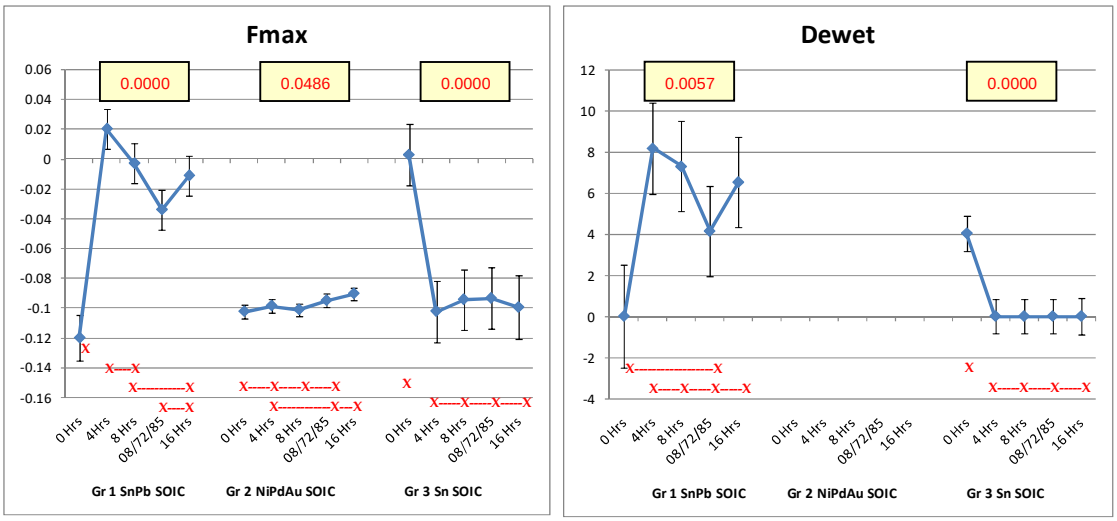
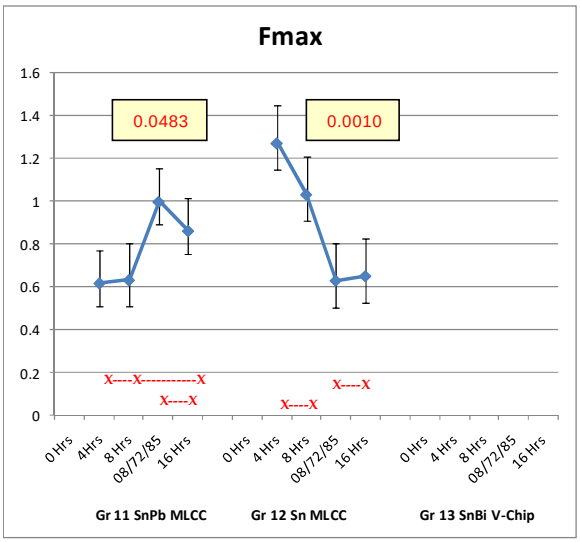
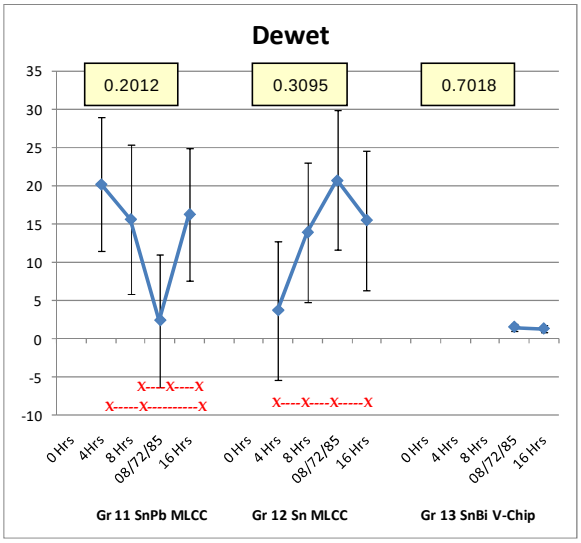
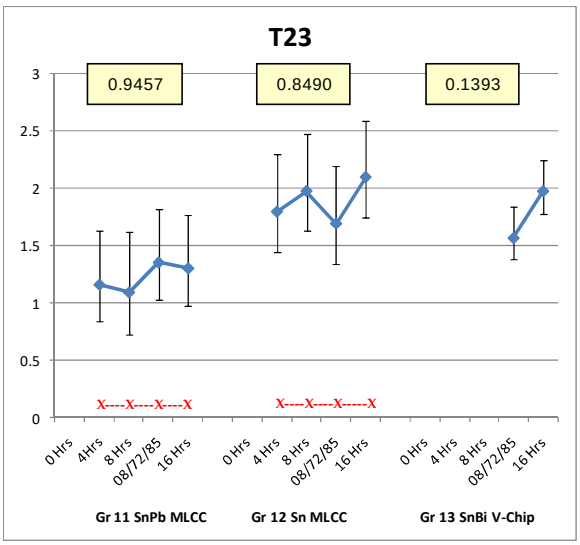


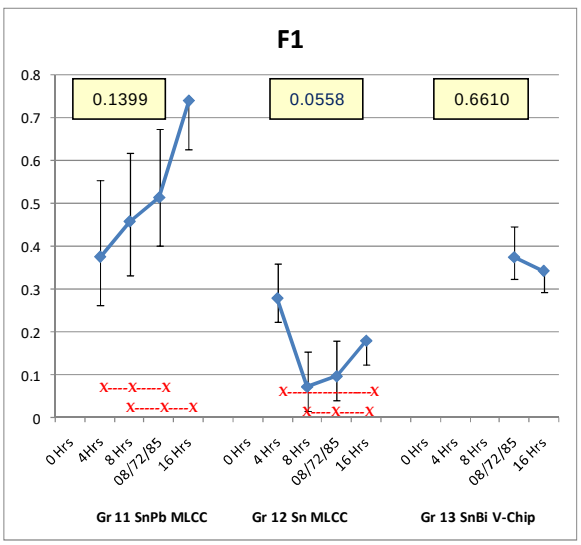
*Figure 5 – Experiment 1 test results for test Groups 9 and 10, the resistor networks*

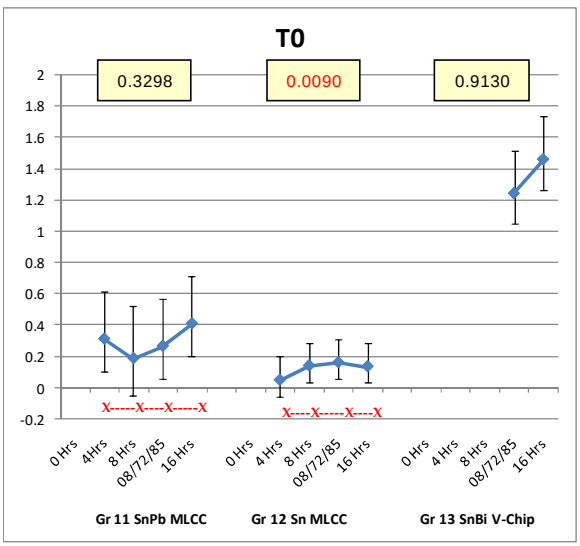
*Figure 6 – Experiment 1 test results for Groups 11 to 13, the MLCC and V-Chip*



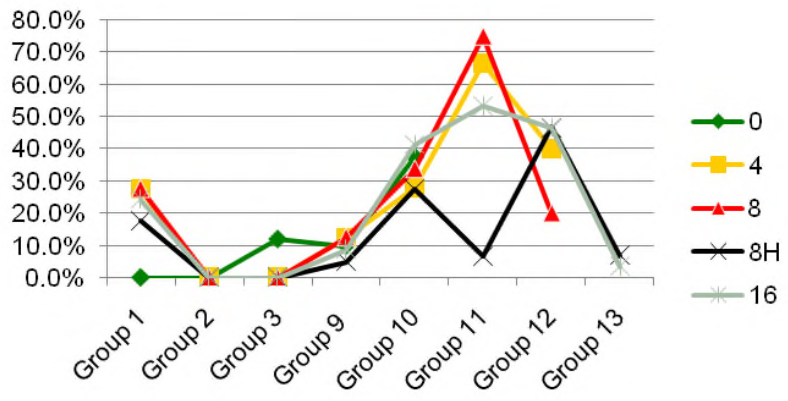
Dewet Results

No preconditioning method appeared to dominate the results. Sn finishes (group 1, 10, 11) appeared to degrade the most. One unusual set was group 12 which was a SnPb surface finish on a SMT capacitor.

*Table 4 – Experiment 1 Dewet Results*

| | Percentage Failing Parts<br>Preconditioning Conditions | | | | |
|---|---|---|---|---|---|
| Sample | 0 | 4 | 8 | 8H | 16 |
| Group 1 | 0.0% | 27.4% | 27.6% | 17.6% | 24.4% |
| Group 2 | 0.0% | 0.0% | 0.0% | 0.0% | 0.0% |
| Group 3 | 12.0% | 0.0% | 0.0% | 0.0% | 0.0% |
| Group 9 | 10.0% | 12.5% | 12.5% | 5.0% | 8.8% |
| Group 10 | 37.5% | 27.8% | 33.8% | 27.5% | 41.3% |
| Group 11 | | 66.7% | 75.0% | 6.7% | 53.3% |
| Group 12 | | 40.0% | 20.0% | 46.7% | 46.7% |
| Group 13 | | | | 6.9% | 3.6% |

*Figure 7 – Experiment 1 Dewet Results*




## Experiment 2 – Confirmation Runs

The purpose of Experiment 2 was to build on the results of Experiment 1, conducting additional selected test runs to confirm the results of Experiment 1. The goal of these round robin tests was to identify an alternative conditioning methodology more applicable to the wide range of component and board finishes encountered today.

The experimental variables, the response parameters, test group numbers, test methods and parameters are all identical to Experiment 1.

The following confirmation runs were performed.

*Table 5 – Experiment 2 Confirmation runs*

| Confirmation Run Parameters | | | |
|---|---|---|---|
| Temperature (◦C) | 215 | 245 | 255 |
| Component A | SOIC Groups 1, 2, 3 | | |
| Component B | 16 Pin DIPS Groups 9, 10 | | |
| Precondition | As Rec'd, 4hrs, 8hrs, Steam | | |

Three different solder temperatures were tested. Five different component types were used and subjected to four different preconditioning methods. All were measured on the wetting balance. A visual examination was conducted to estimate dewet areas.

Experiment 2 – Summary Results

**Solder temperature** - Results at 245°C and 255°C are similar and both are significantly better than 215°C. Because of broad industry use of 245°C, it was recommended for use in solderability evaluation.

**Aging conditions** - Air aging for two years has the smallest influence on component solderability results of any aging method. Solderability results for steam preconditioned components were the most erratic compared to other aging methods, and thus the most difficult to interpret. A recommendation of 4 hours of dry preconditioning was proposed because results were similar to 8 hours and both yielded less variability than steam preconditioning.

Experiment 2 – Detailed Results

Table 6 shows a summary of the significance tests performed on the wetting balance test results collected from the confirmation runs. A “Y” indicates that the wetting balance results for that parameter differed when different “Aging”, or preconditioning, methods were used. An “N” indicates that the results did not differ significantly when different preconditioning methods were used. A p-value of 0.05 or 5% or less was used to determine significance.

For example, looking at G1 (Group 1, SOIC components) parts under the Aging section (where different preconditioning methods were compared), when measuring T0, the table shows an “N.” Thus the T0 results did not differ between the different preconditioning methods. But looking down at the T2/3 results, we see a “Y”, therefore the preconditioning method did influence the results on the SOIC parts when T2/3 was measured.

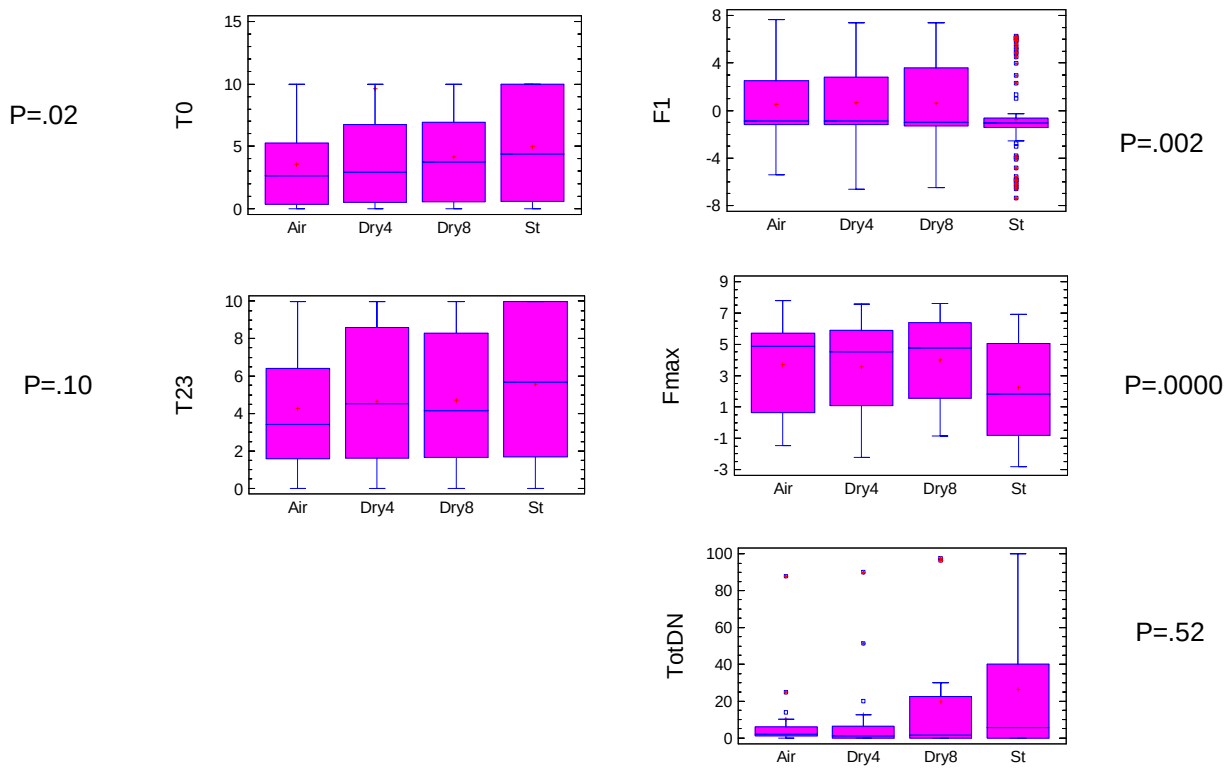
Table 6 – Summary of Experiment 2 Significance Tests on the Dewet Data

| | Aging Method | | | | | Solder Temperature | | | | | Interaction | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | G1 | G2 | G3 | G9 | G10 | G1 | G2 | G3 | G9 | G10 | G1 | G2 | G3 | G9 | G10 |
| T0 | N | N | Y | N | Y | Y | Y | Y | Y | Y | N | Y | Y | N | Y |
| F1 | N | N | N | Y | Y | Y | N | Y | Y | Y | N | N | N | Y | Y |
| T2/3 | Y | Y | N | Y | Y | Y | Y | Y | Y | Y | Y | Y | N | Y | Y |
| Fmax | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | N | Y | Y | N |

Note: significance was judged at the 5% level.

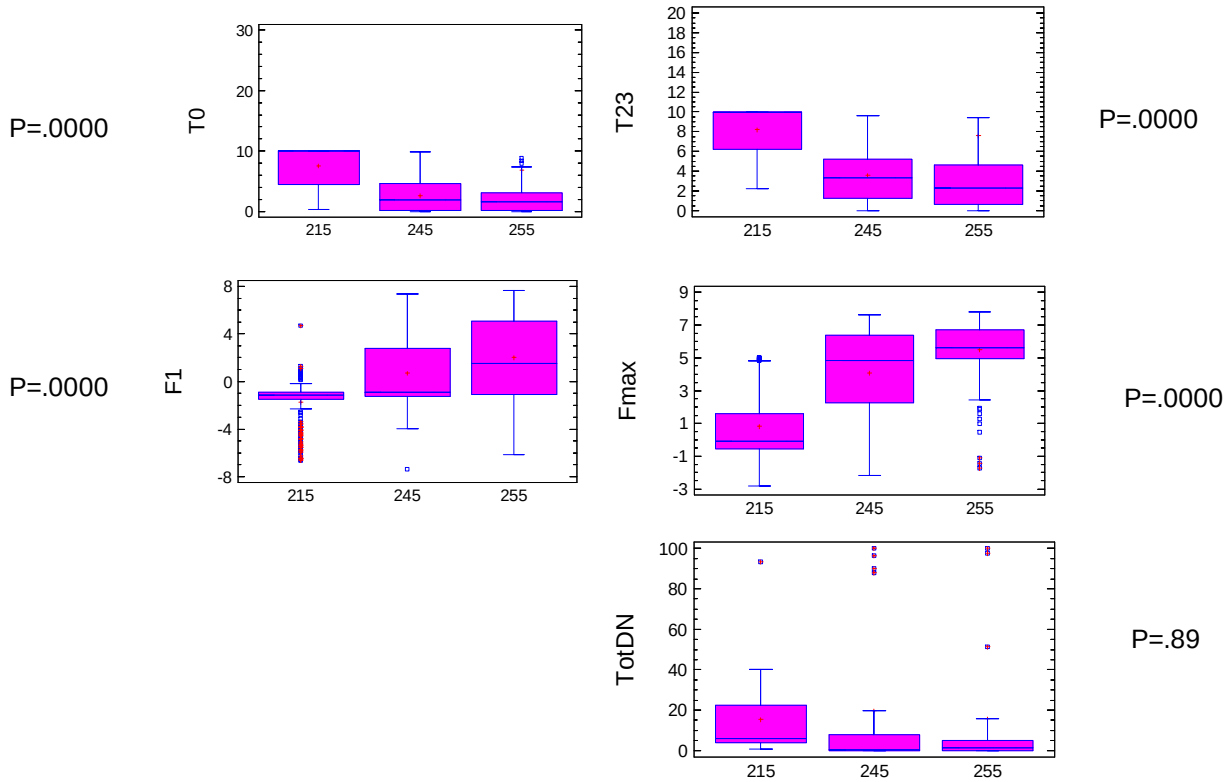
Figure 8 shows a graphical summary of results for the overall data set. P-values are shown next to each graph. These are results of ANOVA F-tests on the test groups and show the probability that the differences between the preconditioning methods could occur due to random chance alone. A p-value of 0.05 or less is usually considered significant.

*Figure 8 – Experiment 2 Overall Results for different preconditioning*



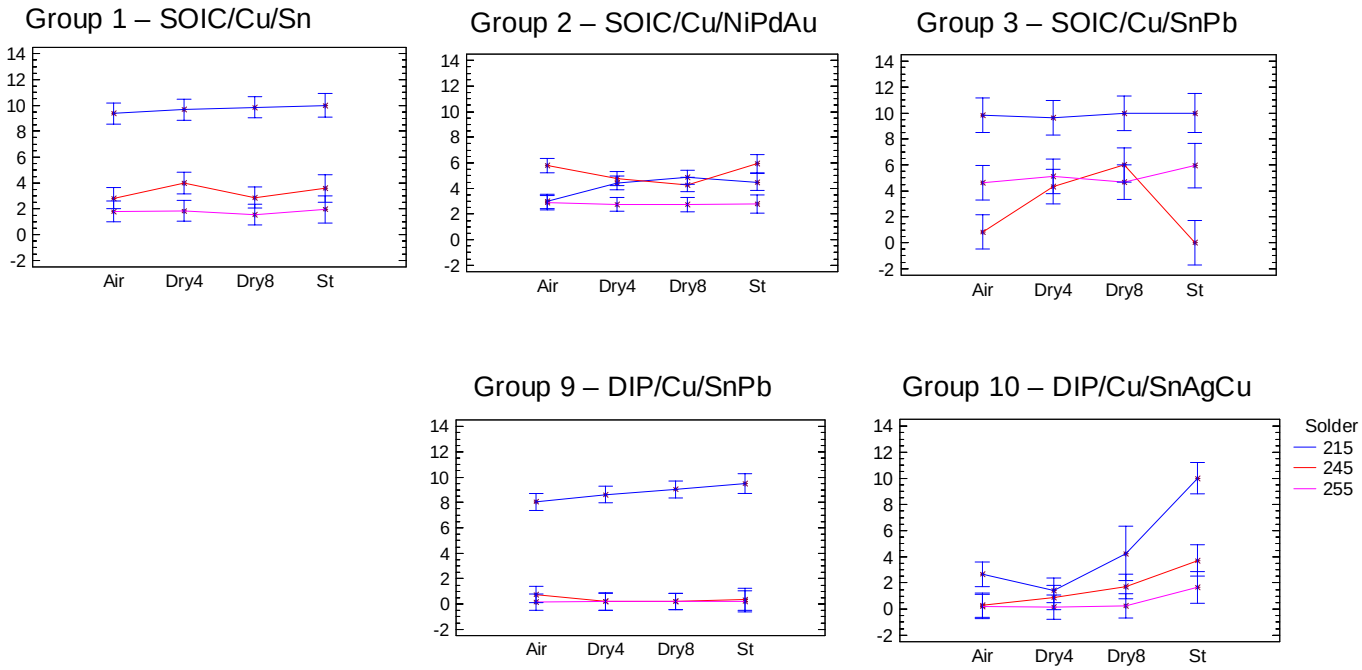

In general, steam conditioning was most severe and air aging was the least severe. Dry 4 and dry 8 conditioning were often very similar in their effects. F1 was not an effective performance metric.

*Figure 9 – Experiment 2 Overall Results for different solder temperatures*



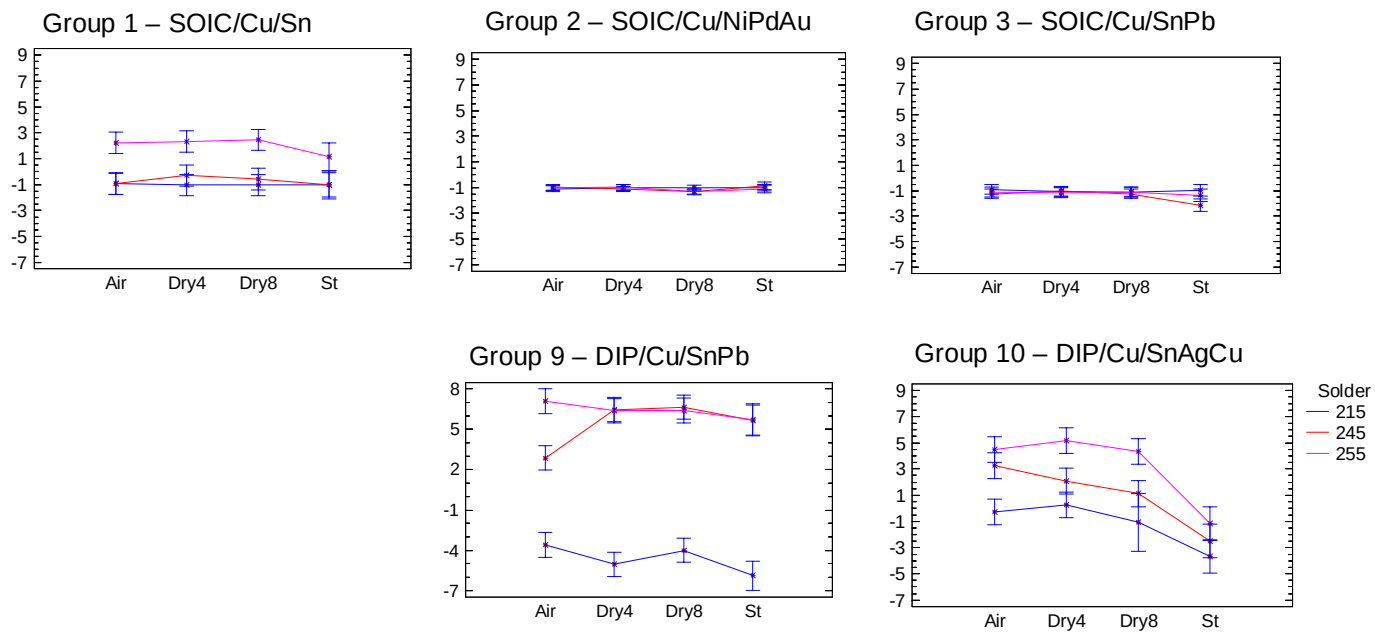

In general, these results showed poorer results at 215°C, and better results at 255°C. Note the presence of many outliers and much scatter/noise. This was a common, but disturbing occurrence in soldering testing, and should motivate further experimentation to find the source.

*Figure 10 – Experiment 2 test results for T0*



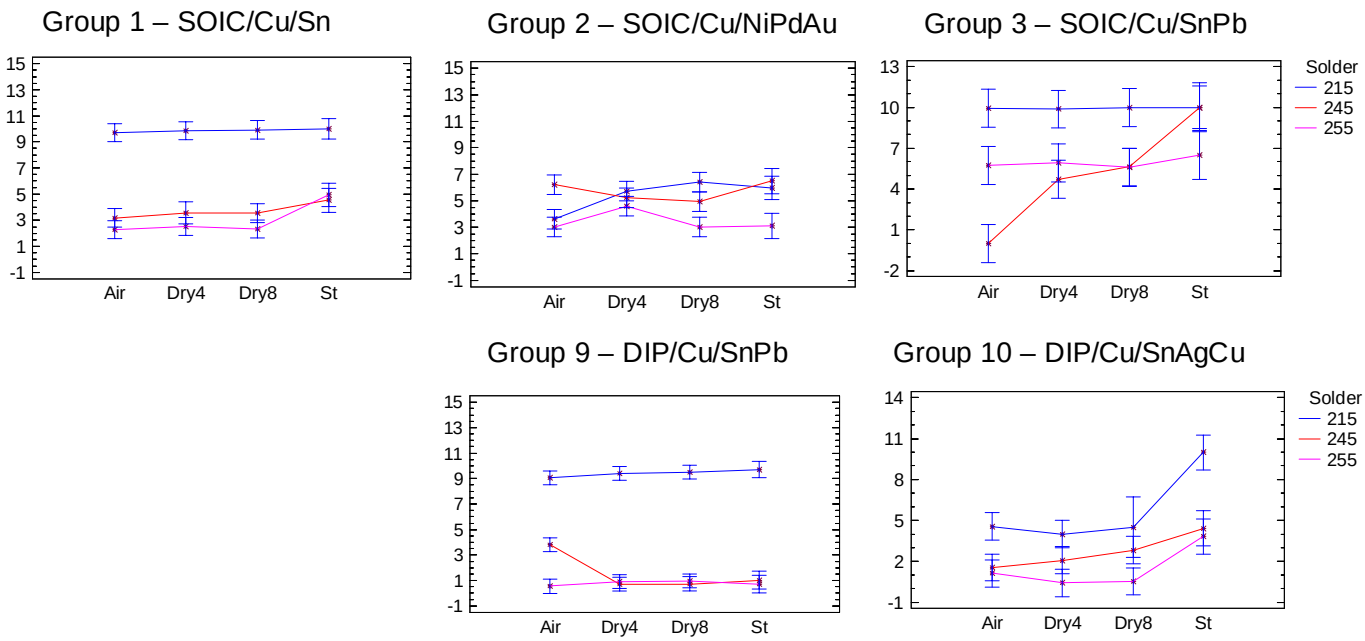

Comments: Poor results at 215°C . NiPdAu and Sn not greatly influenced by conditioning. Results were very similar after 4 or 8 hours of dry conditioning, in most cases.

*Figure 11 – Experiment 2 test results for F1*



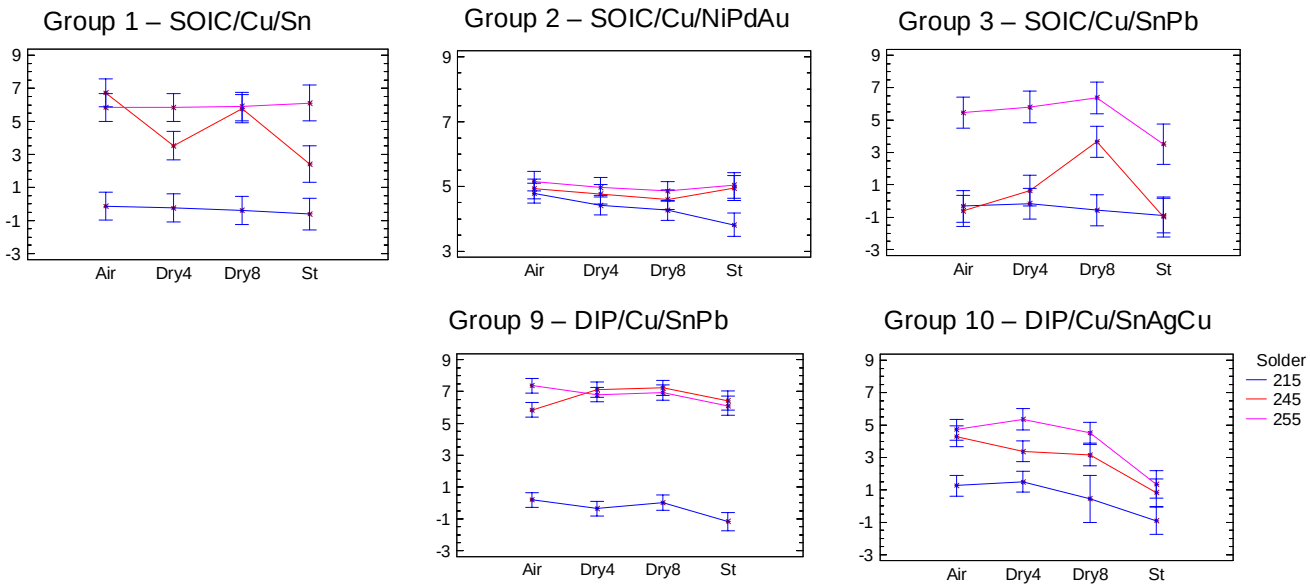
Comments: SOICs didn't solder after 1 sec, except Group 1 at 255°C. Group 9 DIP performed well in all conditioning treatments for solder temperatures 245°C to 255°C. Group 10 DIP using SAC performed poorly after steam conditioning.

*Figure 12 – Experiment 2 test results for T2/3*



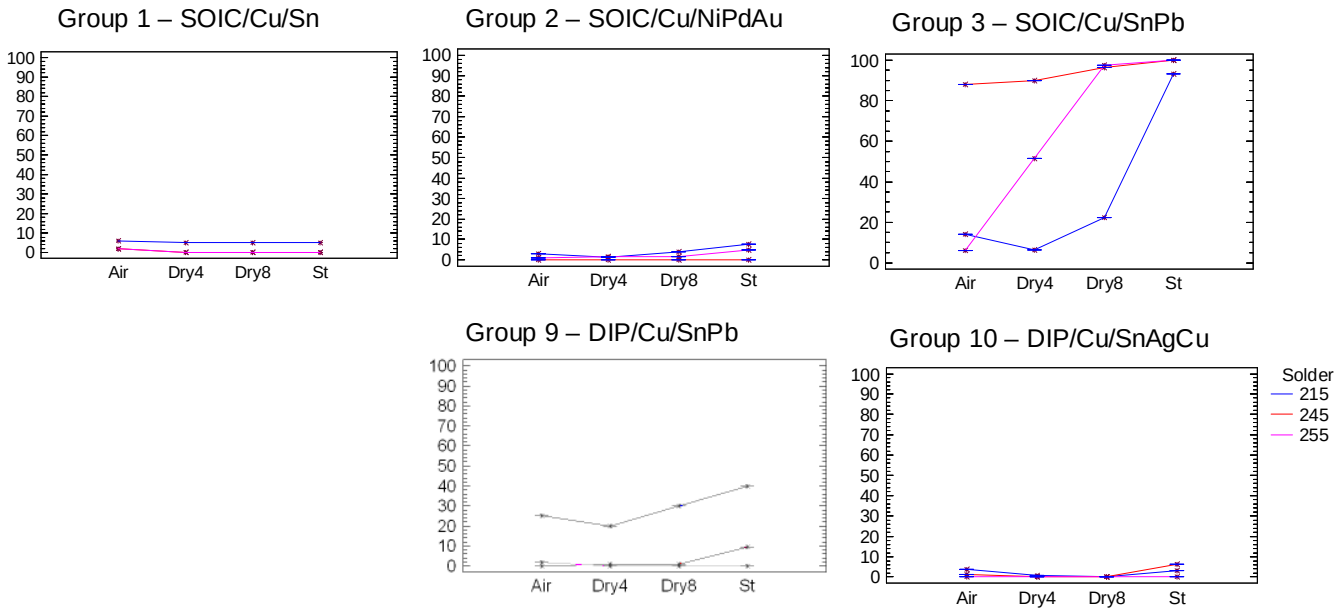

Comments: Poor results at 215°C NiPdCu, Sn, SnPb not influenced by conditioning. Results were very similar after 4 or 8 hours of dry conditioning, in most cases.

*Figure 13 – Experiment 2 test results for Fmax*



Comments: Poor results at 215°C. Inconsistent results for dry 8 results for Groups 1 and 3. Results were very similar after air, 4 or 8 hours of dry conditioning, in most cases.

*Figure 14 – Experiment 2 test results for Dewet Area*




•Dewet/nonwet reported as percent of leads < 95% coverage on the critical areas

Comments: Dewet/nonwet increases in steam. Group 3 results should be reviewed. Sn, NiPdAu not influenced by aging.

## Experiment 3 – The Final Model

The purpose of Experiment 3 was to build on the confirmation data from Experiment 2. The intent was to supplement the known data with some additional test runs to allow further analysis of two important issues:

- How does the solder temperature effect the measured solderability performance when the effects of other known variables are controlled or accounted for?
- Confirm the suitability of dry conditioning to replace steam conditioning.

Two sets of test samples and the following test conditions were used in this experiment:

- The first data set - SOICs and DIPs conditioned in air, steam and dry conditioning for 4 or 8 hours at 150◦C.
- The second data set tested SOICs and 0805 caps conditioned in air and dry conditioning at 155◦C for 12 hours.

Response variables included both the wetting balance and dip-and-look test for both sets of samples.

The following experimental variables shown in Table 7 were included in this experiment. There were 536 results from the test lab G and 2535 from test lab PB.

*Table 7 – Experimental variables for Experiment 3*

| Variable | Levels | Symbol |
|---|---|---|
| Package styles | SOIC, DIP16, 0805 | Package |
| Solder temperatures | 235, 245, 255 | Temp |
| Solder types | Sn63, SAC, Sn | Solder |
| Flux types | 0.002, 0.005% | Flux |
| Conditioning methods | Air, Dry4, Dry8, Dry12 | ID |
| Test labs | G and PB | Source |

Experiment 3 – Summary Results

The two factors which had the greatest influence over the measured solderability of these components were:

- The test lab used
- Package style

The conditioning method had a measurable effect on the solderability.

- Air aging was the most benign
- Dry conditioning appeared to be a suitable substitute for steam conditioning

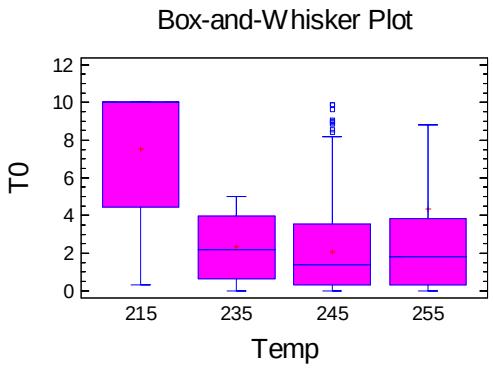
The large number of outliers in the data and the large unaccounted-for variation in the analysis indicated that component solderability continued to be plagued by special causes of variation – the wording of the test method would be important in order to limit or eliminate undesirable causes of variation.

Solder temperature, within the range of 235◦C to 255◦C had a measurable, but lesser effect on the test results.

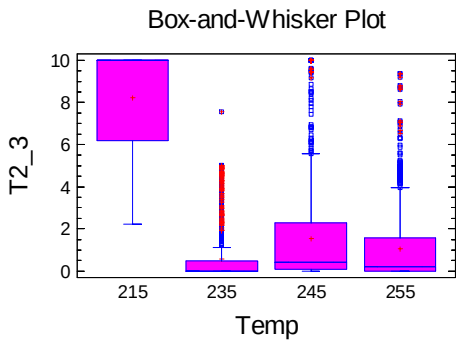
Substituting 245°C for 255°C created a comparable, if slightly more conservative test result.

Experiment 3 - Detailed Results

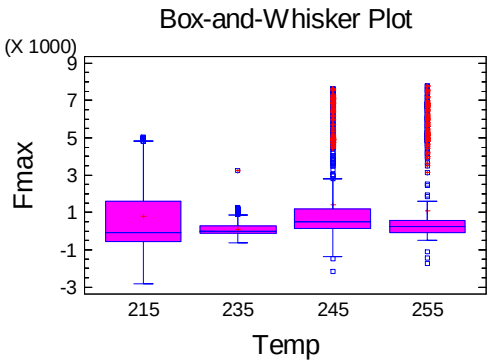
*Figure 15 – Overall Experiment 3 test results by solder temperature*




P=0.3340




P=0.0000




P=0.0000

Comment: P-values show result of significance test. P-value less than 0.05 show significantly different results among test groups.

*Figure 16 – Overall Experiment 3 test results by solder temperature for the two different test labs*

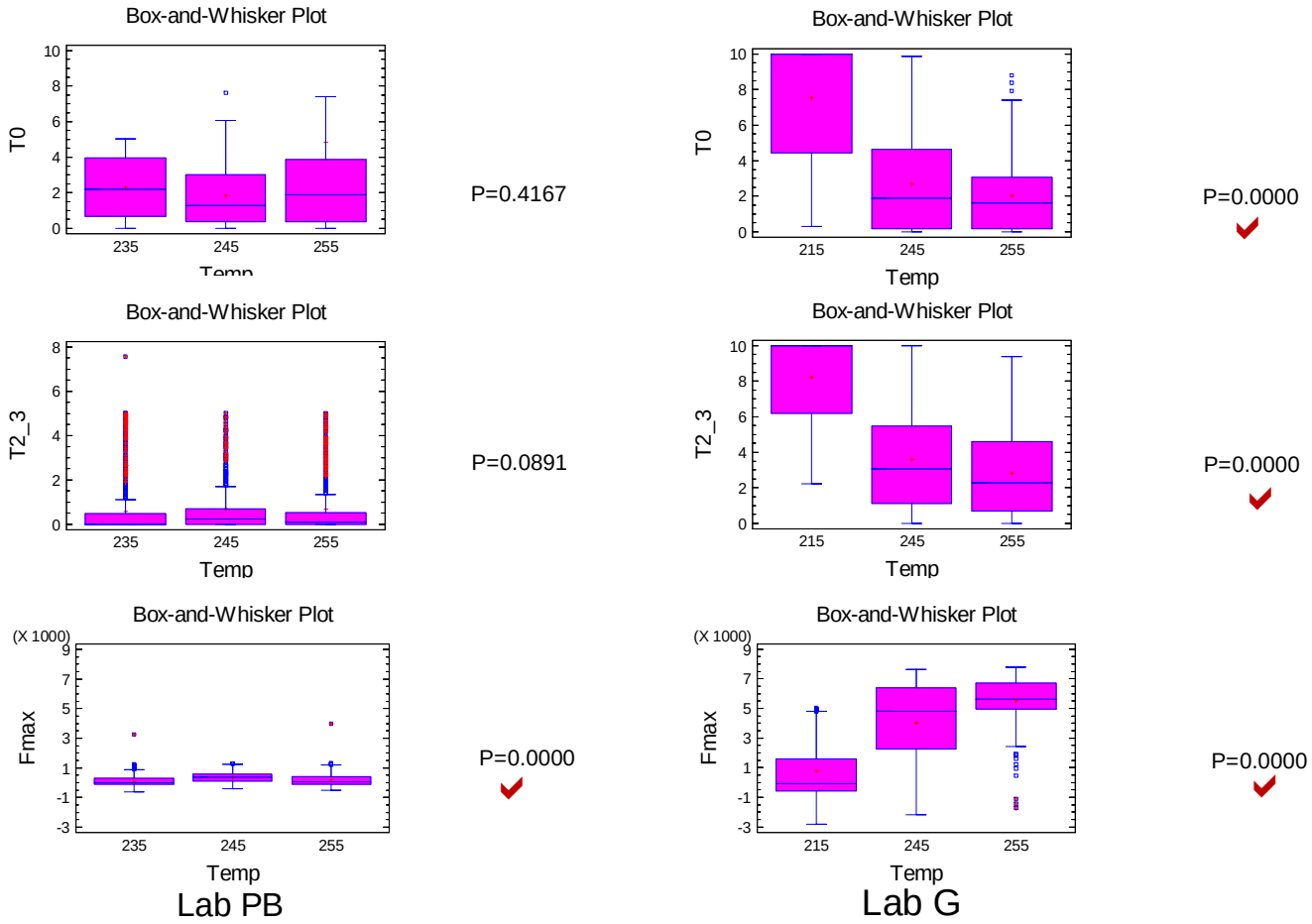
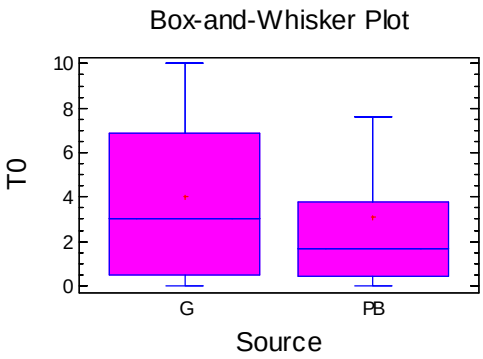
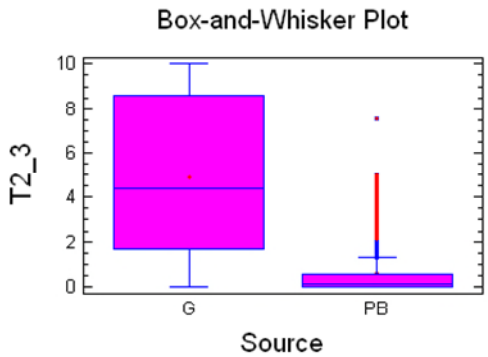


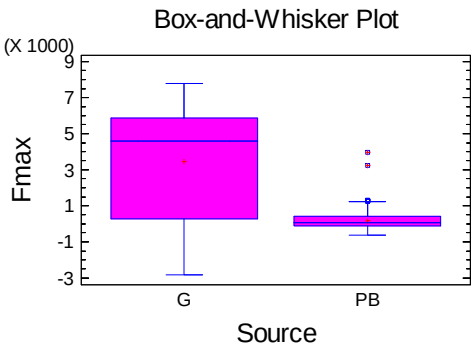
*Figure 17 – Overall Experiment 3 test results for the two different test labs*




P=0.6249

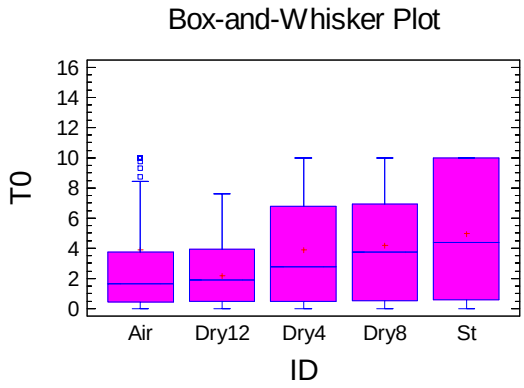



P=0.0000

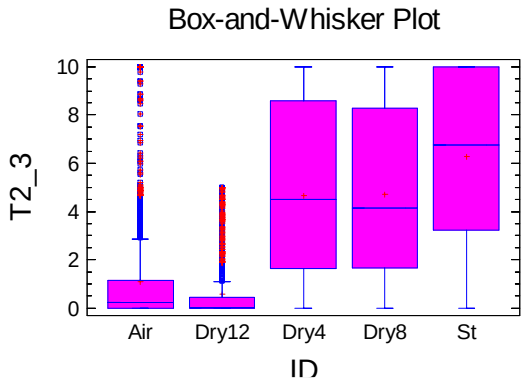



P=0.0000

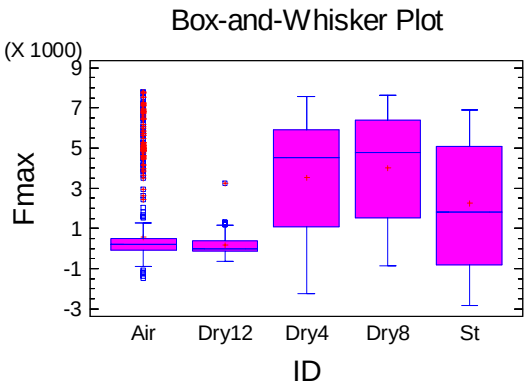
*Figure 18 – Overall Experiment 3 test results for the different preconditions*




P=0.8600




P=0.0000




P=0.0000

General Linear Models -

This data was analyzed using a general linear statistical model relating the wetting balance parameters to the six predictive factors.

Summary of the nested GLM ANOVA test results – Below is a summary of the significance tests on the experimental results. A check indicates a significant factor. The double check indicates the strongest effect.

*Table 8 - Summary of the Experiment 3 GLM Results*

| Source | T0 | T2/3 | Fmax |
|---|---|---|---|
| Package style | | ✔ ✔ | ✔ |
| Test lab | | ✔ | ✔ ✔ |
| Conditioning | | ✔ | ✔ |
| Solder type | | ✔ | ✔ |
| Solder Temp | | ✔ | ✔ |
| Flux type | | ✔ | ✔ |
| Model | | ✔ | ✔ |

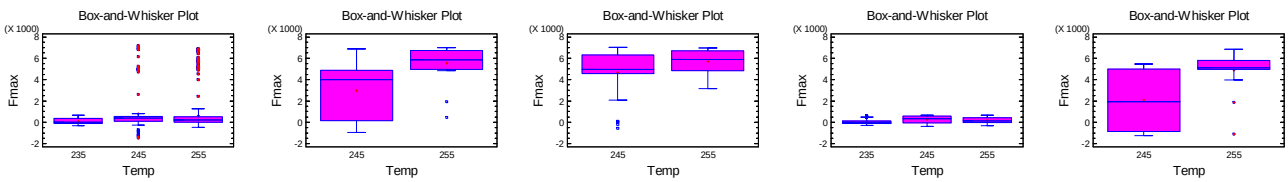
Summary - Test location or package style were usually the most important effects. There was too much variation in T0 measurements to see any clear trends.

Note - Each test location used a different measure of solder force (F1 vs F2), so complete analysis on this parameter was not possible.

In the charts below, a check mark indicates a significant difference between the sample groups, and a circle with a line through it indicates no test data was available.

Figures 19 through 27 contain charts summarizing results for Experiment 3.

*Figure 19 – Experiment 3 test results for Fmax on the SOICs*




Air conditioning ✔

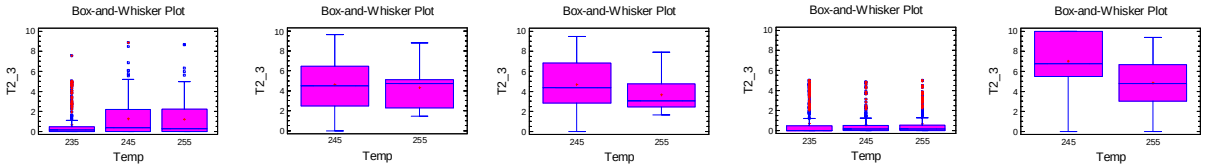
conditioning 150C, 4 hours ✔

conditioning 150C, 8 hours ✔

conditioning 155C, 12 hours ✔

Steam conditioning 8 hours ✔

*Figure 20 – Experiment 3 test results for T2/3 on the SOICs*




Air conditioning ✔

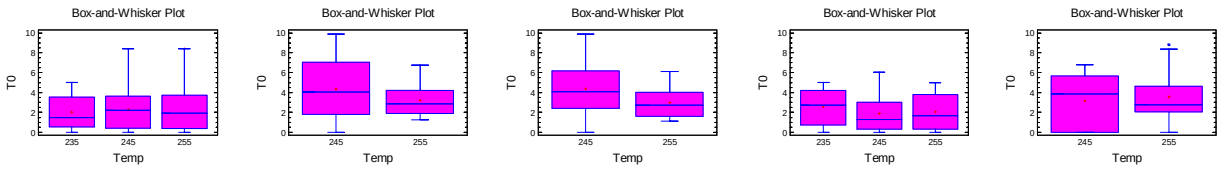
conditioning 150C, 4 hours

conditioning 150C, 8 hours

conditioning 155C, 12 hours

Steam conditioning 8 hours ✔

*Figure 21 – Experiment 3 test results for T0 on the SOICs*




Air conditioning

conditioning 150C, 4 hours

conditioning 150C, 8 hours ✔

conditioning 155C, 12 hours ✔

Steam conditioning 8 hours

*Figure 22 – Experiment 3 test results for Fmax on the 805s*


Air conditioning ✔

conditioning 150C, 4 hours

conditioning 150C, 8 hours

conditioning 155C, 12 hours ✔

Steam conditioning 8 hours

*Figure 23 – Experiment 3 test results for T2/3 on the 805s*


Air conditioning

conditioning 150C, 4 hours

conditioning 150C, 8 hours

conditioning 155C, 12 hours ✔

Steam conditioning 8 hours

Note: The circle with a line through it indicates data was not available for that condition.

*Figure 24 – Experiment 3 test results for T0 on the 805s*


Air conditioning ✔

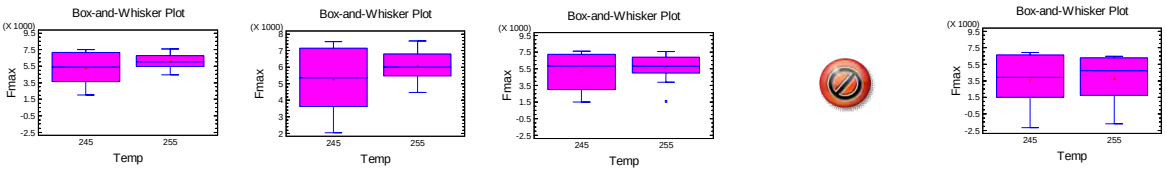
conditioning 150C, 4 hours

conditioning 150C, 8 hours

conditioning 155C, 12 hours ✔

Steam conditioning 8 hours

*Figure 25 – Experiment 3 test results for Fmax on the DIP16s*




Air conditioning ✔

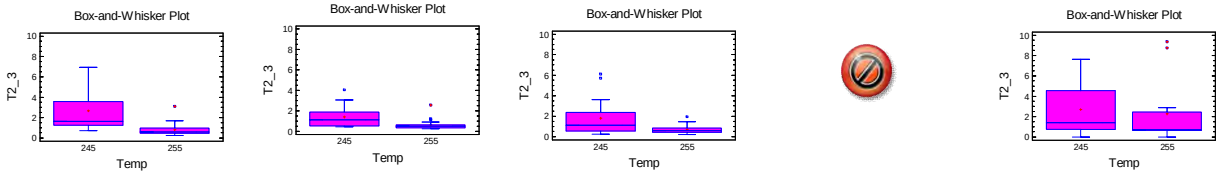
conditioning 150C, 4 hours

conditioning 150C, 8 hours

conditioning 155C, 12 hours

Steam conditioning 8 hours

*Figure 26 – Experiment 3 test results for T2/3 on the DIP16s*




Air conditioning ✔

conditioning 150C, 4 hours ✔

conditioning 150C, 8 hours ✔

conditioning 155C, 12 hours

Steam conditioning 8 hours

*Figure 27 – Experiment 3 test results for T0 on the DIP16s*


Air conditioning ✔

conditioning 150C, 4 hours ✔

conditioning 150C, 8 hours ✔

conditioning 155C, 12 hours

Steam conditioning 8 hours

Note: The circle with a line through it indicates data was not available for that condition.

## Summary/Conclusions

Results of Experiment 1 showed that no one preconditioning method dominated the observed results. This was a positive result, given the number of component types and finishes evaluated. From a high level, the “as-received” components performed better than preconditioned units. In comparing the various lead finishes, both Tin (Sn) and Tin/Silver/Copper (SAC) finishes degraded more than tin/lead (SnPb) finishes. Preconditioning at 155°C for either 4 hours or 8 hours showed to be a better discriminator compared to the other preconditioning options.

In Experiment 2, confirmation runs were performed using 3 solder temperatures, 5 component types and four preconditioning methods. Results using solder temperatures of 245°C and 255°C were similar and results at those 2 temperatures were both significantly better than at 215°C. Solder temperature of 245°C is recommended because of broad industry use. For preconditioning, room air exposure for 2 years (e.g. natural aging) had the least impact on component solderability results. Steam preconditioning showed the most erratic results of the methods. A 4 hours dry bake preconditioning step was recommended because results were similar to 8 hours dry bake preconditioning and either of these yielded less variability than steam preconditioning.

Experiment 3 was performed to build on the confirmation data from Experiment 2. Additional test runs were performed to determine the effect of the solder temperature when the effects of other known variables were accounted for. Experiment 3 was also intended to confirm the suitability of dry preconditioning to replace steam preconditioning. Experiment 3 indicated that the 2 factors which had the greatest influence over the measured solderability of these components were the test lab used and package style. Results also showed that for the conditioning methods, Air aging was the most benign and Dry Bake preconditioning was a suitable substitute for steam preconditioning. Solder temperature, within the range of 235°C to 255°C had a measurable, but lesser effect on the test results. Substituting 245°C for 255°C created a comparable, if slightly more conservative, test result.