



# COMPONENT BULLETIN NO. 11

GUIDELINES FOR THE SURFACE MOUNTING  
OF MULTILAYER CERAMIC CHIP CAPACITORS

AUGUST 1986

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*Engineering Department*

**ELECTRONIC INDUSTRIES ASSOCIATION**

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# GUIDELINES FOR THE SURFACE MOUNTING OF MULTILAYER CERAMIC CHIP CAPACITORS

## 1.0 SCOPE AND INTRODUCTION

This document provides guidelines for the use of multi-layer ceramic chip capacitors, their design and construction as well as handling, mounting and connection requirements. Use of chip capacitors to construct hybrid microcircuits is a mature technology in widespread use. The use of capacitor chips on printed wiring or printed circuit boards as well as other larger area substrates such as ceramic or porcelainized-steel, is a comparatively new technology generally referred to as SMT, surface mount technology.

The physical and mechanical aspects of the chip and its use are the primary subjects of this document. Included is a review of the design and materials employed in the chip's construction, as well as the material and process requirements for their mounting and interconnection by soldering.

Guidelines for the selection and use of these chips based on electrical ratings, values and performance characteristics are given in EIA specification EIA-198-C, Ceramic Dielectric Capacitors.

Note that this document concentrates and directs its information to the mounting and interconnection of chips by soldering.

## 1.1 PURPOSE

The information is provided to assist the user's various engineering and manufacturing personnel in the making of informed choices in regard to these chip capacitors; their selection, specification and circuit assembly processing.

## 1.2 GENERAL CLASSIFICATION OF CIRCUITS AND COMPONENTS

Four general classifications of circuits and components are generally recognized. These classifications are not only determined by the implications of the user's requirements, but also by the characterization of both the components' and circuits' design, construction and implementation. The definitions and remarks which follow for these four classifications are oversimplified. Numerous applications fit between or include aspects of two or more classifications.

### 1.2.1 CONSUMER ELECTRONICS

Consumer electronics in general includes all electronics sold directly to the individual consumer. Circuit function and reliability may be affected by cost considerations, practicality and in some instances, miniaturization requirements. The goal of designers is to provide circuits both of high quality and value and at the same time affordable. This equipment or devices may be characterized by the user's tolerance to failure. For the more expensive products repair is tolerated although reliability is highly valued.

Nevertheless, compromises are made in regard to performance, quality and operational reliability in regard to component specifications, circuit designs and process-assembly techniques. This equipment sector may be characterized by the overriding requirement to be cost efficient due to a high level of competitiveness.

### 1.2.2 INDUSTRIAL ELECTRONICS

Industrial electronics includes a large variety of equipment which is typically not supplied directly to individual consumers. In this category falls most of the equipment in the computer-information processing sector, the communications sector, instruments and controls, and various industrial or process equipment. The components and circuits in general require a higher level of performance, reliability and overall quality than consumer electronics, but for only a small marginal cost increase. The circuit design, component selection and assembly process reflect greater care and effort to minimize the risk of failure. Industrial electronic equipment is expected to have greater operational stability and reliability even with typically more complex and larger circuits in a unit of equipment. Failure costs often are very significant and are not well tolerated.

### 1.2.3 MILITARY AND AEROSPACE

Military specifications exist for the purpose of standardization of component and equipment needs, while at the same time controlling vendors and their product quality, operational characteristics and reliability. Component specifications generally are of the established component failure rate type requiring vendors to maintain testing programs which demonstrate achieved failure rate levels. These specifications may also require additional manufacture lot testing as well as additional 100% screening programs. These components carry a significantly higher cost than consumer or industrial sector components.

#### 1.2.4 HIGH RELIABILITY ELECTRONICS

These components and equipments are found in preceding sectors but are different in that the utmost in reliability is the overriding requirement. This is due to the very high cost of failure such their use in non-redundant life support systems.

The components specified are similar to those in the industrial or military sectors in regard to ratings and performance or stability requirements. The major differences are in the basic design, tighter controls on processes and added specification requirements in regard to part and lot inspections as well as added documentation. The components often reflect conservative design for their ratings. Value ranges are often less per size than in the other sectors.

These High Reliability components and circuits have significantly higher costs than all other types.



## 2.0 CERAMIC CHIP CAPACITOR CONSTRUCTION AND DESIGN

Multilayer ceramic chip capacitors are constructed from many different ceramic dielectric compositions. These compositions are different even for the same dielectric performance characteristic. Internal electrodes and external terminations similarly are of various metals and alloys. They are constructed with at least two dozen major assembly steps. Various manufacturers may employ significantly different construction processes.

The most common ceramic dielectrics are barium titanates. Less common are dielectrics based on other titanates such as strontium or magnesium titanates. Niobates are also used. High frequency capacitors are also made in low dielectric constant formulations from porcelains or vitreous enamels. These types are specialty types for applications requiring the highest Q from VHF to microwave frequencies.

A basic differentiation in the construction process of the chips is based on the manner in which the green, unfired chip is built up. There are two basic methods, the "wet process" and the "dry process".

The wet process consists of building up the capacitors in multiple layers one layer at a time. The ceramic layers are built up by the application of ceramic pastes or inks. Layers containing the electrode sites are similarly built up by the use of metal bearing inks. Electrode patterns are screened over the dried ceramic layers previously laid down. The dielectric is screened or applied over the electrodes and dried. The process is repeated until the desired number of layers is built up. The resulting plate is dried and diced into the individual green capacitor chips.

The dry process builds the capacitor from sheets or films of dried ceramic. These sheets are printed with the electrode inks, stacked and laminated into a plate of the appropriate number of required layers. This method requires the tape casting of the dielectric as an initial step. As in the wet process the resulting multi-element plate is diced into individual capacitors before high temperature firing.

### 2.1 INTERNAL DESIGN

The finished chip consists of multiple layers of internal metal electrodes separated and encased by the ceramic dielectric. Alternate layers of the electrodes are connected to only one of the chips' end surfaces where they contact the exterior metallization, the end termination. The electrodes are only brought to the surface at the appropriate end, any exposure at the sides is considered to be a defect. The internal electrode region is surrounded top and bottom, and side to side as well as from the opposite termination by the

ceramic dielectric, protecting the capacitance forming region of the chip from the external environment. In the popular size chips as much as 50% of the total chip volume is in the noncapacitance forming regions. For significant capacitance range extension, the clearance dimensions between the electrodes and the exterior is reduced to the smallest acceptable dimension. Note that commonly electrodes connected to one end termination extend the length of the chip underneath the opposite termination's metallization.

Also to maintain or extend the capacitance value range, the dielectric layers between electrodes are thinned. A 50% reduction in the dielectric thickness, which also permits a larger number of electrode layers within a given chip thickness, results in approximately a 4X increase in capacitance range. The dielectric composition and quality as well as its thickness are major factors in determining the electrical ratings, performance and operational reliability. High reliability chips generally have significantly reduced capacitance value ranges when compared to similarly sized commercial chip specifications.

#### 2.1.1 INTERNAL ELECTRODES

Precious metals (gold, platinum and palladium) and their alloys were commonly employed as the internal electrode metallizations. These noble metals were required to survive the high temperature of sintering without oxidizing and affecting the chemistry of the crystalline dielectric. In more recent years ceramic compositions with adequate sintering at lower temperatures (~1000°C) have been developed which has allowed high percentages of the much less expensive metal silver to be used in the electrodes. Silver content in these capacitor electrodes varies typically from a low of 20% to a high of 80% or more depending on manufacturer and dielectric formulation. Some manufacturers also use nickel electrodes with low temperature fired dielectrics. Other non-precious metal systems may also be employed.

The internal electrode systems discussed above are all examples of cofired chips, that is chips where metallizations for electrodes and ceramics as dielectrics are simultaneously fired into a monolithic structure. A processing variation is non-cofired chips. In this process the ceramic is first fired by itself and electrodes are injected or impregnated into electrode sites at a later time during a much lower temperature process step. These are also non-precious metal electrode type chips. The metal alloys used are typically high lead compositions with melting temperatures at approximately 300°C (570°F) or higher.

### 2.1.2 INTERNAL DESIGN REQUIREMENTS

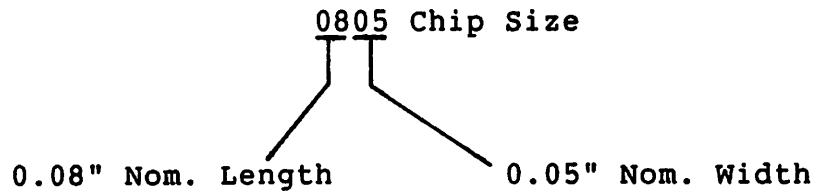
The internal clearance margins, dielectric thickness, uniformity of dielectric and electrode thickness as well as physical defects such as voids, delaminations, cracks, foreign inclusions, discontinuous electrodes, splits, etc. can best be determined by destructive physical analysis. EIA standards EIA-469, Standard Test Method for Destructive Physical Analysis of High Reliability Ceramic Monolithic Capacitors and EIA-510, Standard Test Method for Destructive Physical Analysis of Industrial Grade Ceramic Monolithic Capacitors provide a means of characterizing internal structural features and defects through destructive physical analysis (DPA). This is useful to the user in specifying or testing purchased capacitors to the quality or reliability intent of the circuit design.

### 2.2 THE SIZES, DIMENSIONS, AND VISUAL MECHANICAL REQUIREMENTS

#### 2.2.1 BASICS OF CHIP SIZES

Chips are commonly referred to by a four figure number which relates to the chips length and width. The first two digits designate the nominal length in hundredths of an inch, the second two the nominal width as shown below.

Example:



The other basic dimension, the chips thickness, is typically only specified as a maximum dimension. Usually for smaller chips the maximum thickness is the same as the chip width dimension. For example, the maximum thickness specified for the 0805 chip is commonly .050". Larger chips are typically limited to a maximum thickness of 0.080". The thicker the chip is allowed to be, the greater the capacitance range available in any given voltage rating and dielectric characteristic.

There are at least a dozen different common sizes sourced by U.S. chip manufacturers. This large number results from the special requirements of the hybrid industry over the past several years and reflects sizes commonly available as a function of their use in the construction of leaded, encapsulated ceramic capacitors. The EIA has led the size standardization effort in the U.S. These sizes are detailed in the table which follows. The three smaller sizes, the 0805, 1206 and 1210 account for over 80% of the usage.

These sizes are found in EIA specification RS 198 along with ratings and value ranges in the COG, X7R and Z5U dielectric characteristics. Note that these may be assumed to apply to chips which have their actual thickness close to the specified maximum. In other words, chips which are half the size, half the specified maximum thickness, but retain full ratings and value range may not meet the design intent of the specification in regard to performance and reliability.

#### 2.2.1.1 TERMINATION DIMENSIONS

In the table of dimensions, the width of the termination band on the top, bottom and side surfaces is given as .0275"~.030" (0.7~0.75mm) maximum. This allows for chips which have terminations on the end surface only with no actual termination bands. However, chips are commonly specified with end bands with the typical dimension of .020 ± .010" (0.05 ± .025mm). In many reflow soldering applications, the termination band is the important area for bonding. For wave soldering or other solder immersion techniques, the solder fillet at the end of the chip provides the bond, the termination band is of less importance and may not be required.

Solder coated chips distort the nominal dimensions. An allowance for a .020"~.030" overall chip length increase and an increase of approximately .010" for width and thickness usually must be taken. The solder coating will contribute solder for the fillet joining the termination to the substrate or board mounting pad or band. Non-solder coated chips do not contribute solder to the fillet. Solder plated chips have only a very thin layer of solder or tin and make no appreciable contribution to the fillet.

The actual thickness of the termination metallization is not commonly specified. A single layer of thick film metallization such as palladium-silver is usually less than 1 mil thick at the termination band. It may be somewhat thicker on the end surface. The metallization tends to be thinner over the eight edges of the typical end termination. It is generally thinnest over the four edges connecting the top and bottom surfaces to the sides. These edges are typically called the non-critical edges.

EIA STANDARD SPECIFICATION SHEET  
 FOR  
 MULTIPLE LAYER UNENCAPSULATED CERAMIC  
 DIELECTRIC CHIP CAPACITORS

EIA-198-C

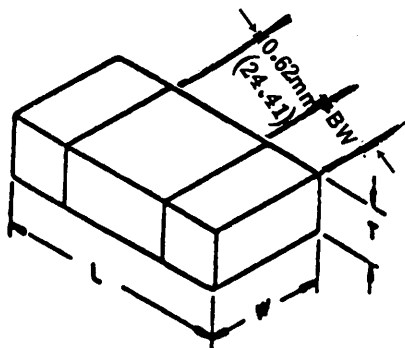


FIGURE 1  
 SOLDERABLE TERMINATION DIMENSIONS

<u>STYLE</u>	<u>LENGTH(L)</u>	<u>WIDTH(W)</u>	<u>THICKNESS(T)</u> <u>MAX</u>	<u>BANDWIDTH(BW)</u> <u>MAX</u>
CC0805	2.0(79) ± 0.2(8)	1.25(49) ± 0.2(8)	1.3(51)	0.7(28)
CC1206	3.2(126) ± 0.2(8)	1.6(63) ± 0.2(8)	1.5(59)	0.7(28)
CC1210	3.2(126) ± 0.2(8)	2.5(98) ± 0.2(8)	1.7(67)	0.7(28)
CC1812	4.5(177) ± 0.3(12)	3.2(126) ± 0.2(8)	1.7(67)	0.75(30)
CC1625	4.5(177) ± 0.3(12)	6.4(252) ± 0.4(16)	1.7(67)	0.75(30)

ALL DIMENSIONS = MILLIMETERS (MILS)

Some termination metallizations are thicker, typically two to three mils thick. Double layers of metallization or barrier layers in the termination are sometimes used. This is usually the price paid to improve the solder leach resistance of the termination. These thicker terminations may help in cleaning by assisting the designer to allow for approximately 5 mils clearance between the chip and board or substrate. On the other hand this thickness must be taken into account where chips are to be glued to the board prior to soldering.

## 2.2.2 VISUAL & MECHANICAL REQUIREMENTS

Chip capacitors which fail to meet the general requirements for material, design or construction may be unacceptable for use in circuit construction or operation. Visual mechanical defects other than basic dimension compliance generally fall into two groupings; termination metallization defects and surface defects in the ceramic. Metallization defects can interfere with proper solder bonding and even affect the capacitors electrical characteristics. Ceramic defects are rejectable because of their potential to provide entry for moisture and contaminants affecting the capacitors reliability. Marking when specified is also a visual examination requirement. There are no standard visual mechanical inspection methods or requirements but general guidelines are given below.

### 2.2.2.1 TERMINATION METALLIZATION VISUAL-MECHANICAL REQUIREMENTS

- A. End surfaces of chips should be completely covered. Small pin holes are generally allowed if the termination will meet solderability test requirements.
- B. The eight edges of the termination are classified as critical and noncritical edges. Critical edges are the four edges which connect the metallization areas of the top, bottom and sides to the end. The four edges connecting the top and the bottom to the sides are the noncritical edges.

Metallization over the critical edges typically has the requirement of no more than 10% failure to cover the edge length due to chipping or failure to cover during metallization. Metallization requirements of the noncritical edges is typically less stringent.

- C. Gaps in the metallization band, except along the non-critical edges, are generally rejected if the minimum band width specification is not met. Extensions of metallization beyond the observed nominal band width similarly are rejectable if the specification limit of maximum band width is not met.

- D. Chip termination bands on each end of the chip should be roughly equal in width. A variation of more than 10 mils from one end to the other may be cause for rejection.
- E. Any obvious blisters in the metallization of greater than .020" should be investigated and may be reason for rejection.
- F. Any foreign material adhering to the metallization which would be sufficient to cause solderability test rejection is not acceptable.

Note that the above examinations are generally only applicable to chips with termination bands, not end only terminations. The distance measurement for band width is generally made from the middle of the inside edge of the metallized band to the end of the chip, which may differ slightly from measurements made only to the edge or shoulder.

The above evaluations are more difficult, if not impossible, to perform on chips which had molten solder coatings applied to the terminations.

#### 2.2.2.2 CERAMIC SURFACE EXAMINATION

- A. Generally cracks in the ceramic if visible under 10X-20X magnification are not allowed.
- B. Holes, voids or spalling in the ceramic are generally not acceptable. If very small, a few mils in diameter, and if obviously they do not penetrate to the electrode layer they may be accepted. Improper laser marking can be responsible for these conditions.
- C. Foreign inclusions visible of more than a few mils in dimension are not acceptable in general. Dark spots or stains which are obvious may also be reason for rejection.
- D. Any chipped or broken edges judged to be greater than 3 mils in depth or which extend for more than 50% of the thickness are rejectable. If there is doubt about any of these chipouts reaching the electrodes it is sufficient reason for rejection. In some chips, electrodes may be buried under up to ten mils of ceramic, in other electrodes may be within a few mils of the surface.
- E. Any exposed electrodes at the sides of the chip or delamination separation at the sides is definite cause for rejection. On polishing, some dielectrics are translucent enough to show indication of internal electrode position even though sufficient thickness of dielectric covers these electrodes.

- F. Any raised blisters or bubbles in the ceramic which extend a few mils beyond the adjacent surface are cause for rejection.

Note that beyond basic dimensional compliance the chips should indeed be brick shaped with parallel surfaces and right angles at surface intersections. Warped, bent, or irregular shaped chips are rejectable even if within basic dimensions if it is judged by the user that these defects will interfere with placement, soldering or reliability in processing. Note also that some chips have rough surfaces under magnified viewing particularly top and bottom surfaces. These chips generally also have sharper edges. Some of these chips even have screening imprints visible. Some chips have edges rounded and have highly polished surfaces. This will vary from vendor to vendor and may even vary from lot to lot.

### 2.2.3 CHIP STRENGTH REQUIREMENTS

Many users are now characterizing or setting requirements for the capacitor chip's strength. This is generally tested by a 3 point beam strength evaluation with a stylus applying force to destruction against the middle of a chip supported on its terminations. The strength of the chip is a function of its physical dimensions and dielectric. The variation in tested strength is due to test repeatability problems, mechanical defect level in the chip and dimension variations in the chip.

The strength of the capacitor of a given length is approximately a direct proportion to its width dimension. The thickness obviously has the greatest effect on strength. It approximately varies with the cube of the ratio of thickness, thicker to thinner. A chip with a .040" (1mm) thickness may be expected to require a break force roughly 4.5 times greater than that of a .024 (0.6mm) thick chip.

Typical elastic properties for chip capacitors with both COG (NPO) and X7R (BX) type dielectrics are a Young's Modulus ranging typically from 18 to 22 Mpsi, a Shear Modulus ranging from 6.5 to 8 Mpsi and a Poisson's Ratio typically 0.33-0.34. The reported measured lows and highs were Young's Modulus from 12 to 32, Shear Modulus from 4 to 12 and Poisson's Ratio from 0.24 to 0.43.<sup>1</sup>

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<sup>1</sup>Michael Cozzolino "Stress Determination for Surface Mounted Ceramic Capacitors," CARTS '86 Proceedings (The Components Technology Institute, Inc., 1986), pp. 42-52.



A broken chip on a circuit board typically exhibits a clam-shell break rarely in the middle of the chip. The break commonly begins at the metallization band edge. These breaks are thought to result from tensile stress and some bending stresses exerted on the chip body through the solder bond. This break, if found, more commonly occurs on alumina ceramics during cooling from soldering. For circuit board mounted chips it may occur on heating previously soldered chips or upon warping or bending the board.

For thinner 1206 chips, the minimum acceptable break force is one kilogram, 2.2 lbs. Thicker chips can be rated at four kilograms, 8.8 lbs., minimum.

### 2.3 CHIP TERMINATION METALLIZATIONS

In the past the majority of chip capacitors have been reflow soldered onto alumina ceramic substrates, more specifically onto palladium-silver alloy mounting pads fired onto the substrate. The chip termination and the substrate pads were commonly of similar metal alloy, a natural fit for the capacitor termination.

The majority of chips today are soldered to solder coated copper circuit lands or pads on the surface of epoxy-glass circuit boards. These chips, whether reflow or flow (wave) soldered, must be suitable for the different processing environment.

Due to these facts, plus the other various mounting methods employed in hybrid circuit construction such as wire bonding and conductive epoxy bonding, there are several termination options available.

#### Typical Termination Metallizations

<u>Type</u>	<u>Surface Metallization</u>
1. Single Alloy/ Metal Metallization	(1) Palladium-Silver, Pd-Ag Silver, Ag
2. Guarded or Barrier Layer (Plated)	(2) Tin [Sn] or Tin-Lead [SnPb] (Ni or Cu barrier layer), or Gold [Au] over Ni barrier, Gold [Au] over Cu barrier, or Nickel
3. Solder Coated(3) Over Type 1. above Over Type 2. above	
4. Solderable Thin Film	

- (1) Palladium is typically 15%-20% of alloy by weight.
- (2) In some cases plated tin or plated tin-lead of a specific alloy type may be preferred. These coatings may be supplied as plated or (on request) reflowed.
- (3) Solder alloy used for coating may vary. Most have molten range below 200°C. Silver bearing solder type SN62 is commonly employed.

Types listed in the table were chosen only for convenience in listing. They are not offered for use in part numbers or specification call outs. EIA specification RS198 offers only one termination description and that is "solderable terminations".

Also there is a termination classification system using the numerals 1 through 3 indicating inherent leach resistance characteristics. Classification 1 is the most leach resistant and classification 3 the least.

In high humidity operating environments, metal migration between terminations is a concern and a known mode of failure for smaller chips. Silver is commonly the culprit as it migrates readily when open to humid environments under voltage potential differences and more rapidly in the presence of ionic contaminants. Solder coatings inhibit this effect if the silver is completely covered and not exposed at the edge of the termination. If exposed, it has been reported that solder coatings may actually accelerate the migration of silver.

### 3.0 CHIP MOUNTING PAD DIMENSIONS

In hybrid circuit manufacturing the metallized sites for chip connection are called pads. In printed circuit board terminology they are commonly called either pads or lands.

The following material presents two different pad designs. One is for reflow soldering the chips using solder paste coated pads as the only source of solder for the joining. The second set of designs are for flow or wave soldered chips. In this case, chips previously glue attached to the board are soldered by immersion in a molten solder wave or bath, no solder paste being required.

#### 3.1 REFLOW MOUNTING PAD DIMENSIONS

Reflow pad dimensions are determined by the chip size, the placement accuracy, and the amount of solder required for an acceptable fillet. Before solder reflow, the chip is held in place by the adhesion of the dried solder paste that coats the pads. Soldering is accomplished by remelting and reflowing the solder present in the paste. If the chips are solder coated, then that solder also contributes to the solder fillet. Solder coating of the chips does not have any significant impact on mounting pad dimensions, although it may have an impact on placement accuracy.

The shape and size of the solder fillet is largely controlled by the amount of solder paste present. This, in turn, is a function of the pad area, the thickness of the paste and the amount of solder by volume contained in the paste.

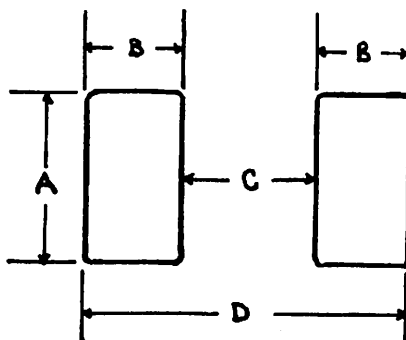
Pad design allows for self-centering or alignment of the chips on the pads during reflow of the solder. The chips have a tendency move to accommodate the forces exerted on it by the surface tension of the molten solder wetting its termination metallization. Movement will seek to balance these forces where possible. This effect may be limited on end only termination designs. If the chips are placed so that they are not totally in the pad areas, this effect may not bring the chip into alignment.

The larger pads which allow for a solder fillet formation along the bottom edges of the chip allow for visual examination of the reflowed bond. Visual examination reveals good bonding or wetting by the shape of the fillet. The surface appearance of the solder fillet is used to examine for grainy crystallized bonds or contaminated bonds.

The reflow pad dimensions and spacings in 3.1.1 assume chip termination bands of  $0.020 \pm 0.010$ " ( $0.5 \pm 0.25$ mm) with additional allowance for a  $0.005$ " ( $0.13$ mm) wider band for the two larger chip sizes.

End only terminated chips, no termination band, may be mounted on the 3.1.1 dimensions. If desired, the C dimension in this case may be increased by  $0.025$  to  $0.030$ " ( $0.6$  to  $0.75$ mm). The B dimension may also be decreased by  $0.012$  to  $0.015$ " ( $0.3$  to  $0.4$ mm).

3.1.1 SUGGESTED REFLOW MOUNTING PAD DIMENSIONS - STANDARD CIRCUIT DENSITY



EIA Chip Sizes	A	B	C	D
	Min.	Min.	Nom.	Nom.
0805	.080" 2.0mm	.050" 1.25mm	.030" 0.75mm	.130" 3.3mm
1206	.090 2.3mm	.050 1.25mm	.075 1.9mm	.175 4.45mm
1210	.130 3.3mm	.050 1.25mm	.075 1.9mm	.175 4.45mm
1812	.160 4.1mm	.060 1.5mm	.120 3.0mm	.240 6.1mm
1825	.285 7.2mm	.060 1.5mm	.120 3.0mm	.240 6.1mm

Comments:

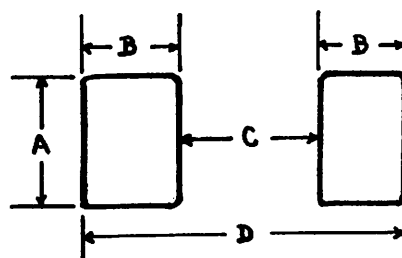
- A. Dimension A allows a minimum of  $0.010$ " ( $0.25$ mm) on each side of a centered chip using max. chip width.
- B. Dimension B allows a minimum of  $0.020$ " ( $0.5$ mm) on each end of a centered chip allowing for maximum chip length.

- C. Dimension C is equivalent to the nominal distance between termination bands minus 0.010" (0.25mm).
- D. If the pads are portions of larger metallized areas, then the pad dimensions should be defined by the use of solder masks or dielectric material coverings.

The pad areas defined above, if covered with 0.008" (0.2mm) of solder paste containing at least 50% solder by volume, will allow for the creation of roughly 45° angled fillets reaching up to about .015" (0.4mm) of the chip thickness, leaving 0.004" (0.1mm) or less solder bonded between the bottom chip band and substrate pad. This fillet height is one half or more of the smaller chip typical actual thicknesses. Larger deposits of solder paste may be used if stencils are used in the screening process. Of course, greater amounts of solder result in large fillets.

3.1.2 SUGGESTED MINIMUM PAD DIMENSIONS FOR HIGH DENSITY MOUNTING

These pads are designed for the use of circuit designs where high density mounting is the overriding requirement. The majority of the solder bond and its strength resides in the visually uninspectable solder bond between the bottom termination surface and the substrate or board pad. Chips with end only terminations are not recommended for these pad designs. This pad design produces a greater solder pedestal effect in chip mounting.



EIA Chip Sizes	A Nom.	B Nom.	C Nom.	D Nom.
0805	.055" 1.4mm	.030" .75mm	.030" .75mm	.090" 2.3mm
1206	.070" 1.8mm	.030" .75mm	.075" 1.9mm	.135" 3.4mm
1210	.105" 2.7mm	.030" .75mm	.075" 1.9mm	.135" 3.4mm

Comments:

- A. Dimension A allows .005" (0.13mm) total over the nominal chip width.
- B. Dimension B allows .010" (0.25mm) total over the nominal chip length.
- C. Dimension C is equivalent to the nominal distance between the chip termination bands minus .010" (0.25mm).

These minimum size pads, if covered with .008" (0.2mm) of screened on solder paste, allow for a solder thickness between the chip termination band on the bottom and the chip pad. Since the solder bonds are not available for visual examination for good quality, highly solderable termination bands, good solder paste and careful soldering techniques must be used.

### 3.2 FLOW OR WAVE SOLDERING PAD OR LAND DIMENSIONS

The chip terminations and the circuit board lands are fully immersed in flowing molten solder. The chips are held in place by glue attachment. This soldering process provides plenty of molten solder to form a fillet. This is a concern because the solder bond strength can exceed the inherent strength of the chip or the chip's termination bond to the ceramic chip body. Stress due to flexing in the circuit board is best accommodated by the solder fillet. The solder fillet size is purposefully limited in good practice to allow it to yield without breaking the chip. Smaller, thinner fillets are obtained by limiting the size of the mounting pad, its width and the length exposed on either end of the chip.

The use of a hot air-knife after solder wave immersion also reduces the amount of solder in the fillet. This permits the use of wider lands without undue concern.

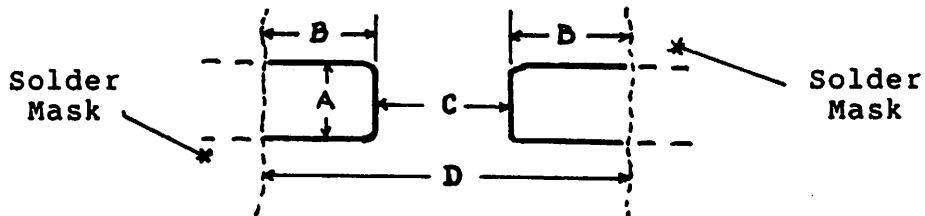
0805, 1206 and 1210 size chips properly soldered to circuit boards will withstand a 0.125" (3mm) deflection of the board across a span of 3.5" centered on the chip mounting. Chips are wave or flow solder bonded to pads described in the following section, 3.2.1, after being glued to the circuit board. Circuit board material is FR4 laminate or similar approximately .062" thick.

There will be no evidence of damage to the chip or the solder band by electrical and visual inspection.

The mounting land layout specified in the following section 3.2.1 is recommended for production wave soldering.

The glue dot or bar must not flow over the edges of the mounting pads or lands. It should be centered on the chip between terminations if applied to the chip before placement. If applied to the board, the glue should be centered between the pads. The glue height, after allowances for slumping, must be of sufficient height to make contact with the chip when placed. The thickness of the boards lands or substrates pads must be taken into consideration as well as the chip's termination thickness. If solder masks or dielectrics are between the pads or lands, particularly if covering other circuit paths, this will also affect the required glue thickness. In some cases a glue height of .003" to .004" (.075-.1mm) will not make adequate contact. In all cases the "squish pattern" of the glue should be taken into account. Too much glue can result in the excessive elevation of the chip from one or both of the mounting pads creating a potential soldering problem. See section 6.2.

3.2.1 SUGGESTED WAVE (FLOW SOLDERING LAND DIMENSIONS)



Chip Size	A	B	C Nom	D
0805	.035-.050	.050-.065	.030	.130-.160
1206	.035-.050	.050-.065	.075	.175-.205
1210	.060-.100	.050-.065	.075	.175-.205
1812	.075-.100	.060-.075	.120	.240-.270

Comments:

- A. Dimension A should be from 2/3 to the full nominal chip width dimension; 0.035" (0.9mm) minimum. A .040" (1mm) is adequate for both .050" (1.25mm) and .063" (1.6mm) width chips, 0805 and 1206 sizes. A .063" (1.6mm) is generally also considered adequate for larger chips to widths of .125" (3.2mm), 1210 size.
- B. Dimension B should allow a .020" to .040" (.05-1.0mm) solderable area exposed at each chip end for access to the flowing solder. The larger dimension is appropriate for thicker chips or chips where the termination is shadowed from solder flow by the chip body or other components.

C. Dimension C is equivalent to the normal distance between termination bands minus .010" (0.25mm).

The lands are portions of larger areas of metallization or conductors and should be defined as described by the use of solder masks or dielectrics. If conductors are run over the board beneath the chips they must be solder masked.



#### 4.0 OTHER MOUNTING & INTERCONNECTION CONSIDERATIONS - SOLDERING

The typical capacitor chip termination has a third or less of the area of a leaded components wire surface area which is used for the soldered connection. While a component pin or lead is mechanically strong, a chip termination consists typically of a thick film metallization which is weaker or prone to fracture under stress. Termination metallization may weaken when it has been attacked by molten solder. Even at circuit operating temperatures termination reliability may be affected by inter-metallics growth with time. The quality of the chip termination is very important. Its solderability, resistance to soldering heat, and leach resistance are key selection factors.

##### 4.1 SOLDERABILITY

(Refer to requirements and test method found in RS-198.)

To effect a good solder joint both electrically and mechanically the soldering conditions must be optimum. The solderability or solder wetting characteristics of the capacitors terminations and of the substrate pads or circuit board lands must be acceptable. The time to wet as well as the degree of surface coverage achieved with a given soldering flux, solder and soldering temperature and time profile are indicative of the termination's basic solderability.

The capacitor chip is tested by fluxing the chip and then immersing it into a solder pot for four or five seconds. After its withdrawal and cleaning, the resulting coating of the termination should be shiny and smooth, free of voids and areas not wet by the solder. Various test specification requirements specify that the resulting solder coating be smooth and continuous allowing defects which are anywhere from 5% to 25% of the termination surface area. A typical test consists of the following sequence:

- A. Aging - 1 to 8 hour exposure to steam from boiling water under normal atmospheric pressure.
- B. Flux Application - Immersion in R type flux for 5 to 10 seconds and allowed to drain for up to a minute at room temperature. (RMA flux may be specified.)
- C. Solder Dip - Immersed in molten solder, SN62 most common, for five seconds; solder temp. at 230° to 250°, 245°C  $\pm$  5° now commonly specified. (Lower temperatures such as 215°C are also employed. Longer immersions are applicable up to ten seconds.)

- D. Cleaning - Remove excess flux in fresh isopropyl alcohol by immersion with agitation.
- E. Visual Examination - Both terminations examined for extent of fresh solder coverage under at least 10X magnification.

Solderability testing where possible should mimic the materials and conditions appropriate for the manufacturing process. The various flow and reflow solder techniques use different solders, solder temperatures, soldering heat durations and solders.

Evaluation of solder fillets produced in manufacturing is also highly recommended to maintain process control and for the production of reliable circuits. Voids in the solder fillets are defects not easily spotted except by destructive tests.

Manufacturer's recommendations on part storage should be followed. Packaging that is opened should not generally be placed back in inventory after being on the production floor. Silver alloy terminations especially require protection from sulphur compound containing materials, requiring special paper and cardboard package materials as well as "silver saver" additives in the packaging. Packaging for chips whether silver, gold or solder terminated also often includes the use of desiccants. Some manufacturers even maintain components with these type terminations in nitrogen-filled storage cabinets to maintain solderability. Chip components should be kept in sealed bags or vials. Sealed bags are good practice even for taped and reeled chips.

A good recommendation to follow is to use chips within six months of their shipment from the manufacturer. Certainly, chips which have been stored for a year or more should have their solderability reevaluated before use. A good practice is to ensure that the chips first into inventory are the first out. Chip packaging should contain shipment date or lot manufacture date information.

Some soldering operations, because of the difficulty of cleaning, use non-activated flux, type R, which requires the terminations to be especially free of oxidation or other contamination. Tin-plated or solder-coated chips are typically used in these more critical soldering applications.

#### 4.2 LEACH RESISTANCE AND EFFECTS OF SOLDERING HEAT (Refer to requirements and test methods in RS-198.)

Hot molten solders, particularly those rich in tin (Sn), cause dissolution of the silver from termination or pad metallizations that can destroy the metallizations or its attachment to the underlying ceramic. This destruction or dissolution is commonly called leaching.

Leaching limits the amount of molten solder exposure or soldering heat that the chip can withstand without significant damage both mechanical and electrical. While chips may be safely soldered into a circuit, repeated exposure for the purpose of rework or repair may damage the chip. The total amount of exposure must be considered to assess potential chip or mounting pad damage.

The use of copper or nickel barrier layers plated over the primarily silver or silver alloy metallization greatly extends the time of solder heat exposure before damage occurs. Care must be taken with silver or silver alloy terminations even if plated with tin or gold to promote solderability. Solder coatings or plating without a barrier layer do not appreciably retard leaching. In fact, solder coating of the chip, which requires immersion in molten solder, reduces the time of molten solder exposure during assembly before leaching of the silver metallization occurs.

The silver terminations suitable for reflow soldering contain approximately 20% palladium in a palladium-silver alloy. This inhibits leaching. A single "coat" of this metallization is typically 0.001" (25 microns) to 0.0015" (38 microns) thick. However, the thickness over the edges of the termination are typically less. These edges and the edge of the termination metallization where it meets the ceramic surface are where the effects of leaching are usually most obvious. Different manufacturers using essentially the same basic materials (and even different lots from a single manufacturer) can display considerable variation in leach resistance. This is the result of material differences and variations in the silver ink application and its subsequent firing.

There are many different test methods in use in the industry for quality conformance testing. Some are based on testing identical to the solderability test except extended for longer immersion times and/or higher solder temperatures. Others are based on mounting chips on substrates and reheating to soldering heat for extended period of time to note changes in the solder fillet indicative of termination leaching. Examination of the fillet is a difficult evaluation. A destructive cross-sectioning of the fillet is required to determine what is going on under the fillet.

For hybrid assembly work using standard belt conduction and tunnel soldering and silver bearing solder with capacitor chips which have palladium-silver terminations, a simple extension of the solderability already described should be a sufficient leach resistance test (see 4.1). Repeat the 5 second solder immersion two or three times while examining its effect on the termination. If a maximum of 25% of the original metallization (other than that on the end surface) has been removed it is generally acceptable. Up to 50% missing metallization over the critical edges, the edges which join the end surface to other surfaces, is also generally acceptable in commercial applications. Requirements for high reliability and military circuits are however more demanding.

For circuit board assemblies, a more critical test is appropriate since both the soldering temperature and time of exposure to soldering heat are likely to be greater than for hybrid assembly.

Again a chip in solder immersion test similar to the method employed for solderability testing may be used. The solder pot temperature should be increased to 260°C and a minimum immersion of ten seconds is recommended, twenty seconds is more appropriate. This test should cover the needs of circuit board soldering using dual-wave soldering machines and machines using infra-red diffuse heating. For soldering by vapor-phase techniques where the temperature is lower, 215°C, but the exposure time is twenty seconds up to two minutes, the longer 60 second immersion is the recommended leach resistance test. For high temperature vapor phase processing only barrier layer or other leach resistance terminations are recommended.

RS198 has included termination classification for chips. Classification 1 terminations are basically highly leach resistance terminations with a solder immersion test time of 60 seconds. Similarly classification 2 test time is 30 seconds, 3 is 10 seconds. Classification 3 is suitable for most hybrid assembly work. Where the other classifications fit the various circuit board soldering requirements has yet to be determined. Classification 3 may prove suitable for dual-wave soldering especially where the solder temperature is controlled to 20°-30°C below the normal temperature of 250°C used in traditional leaded component circuit board wave soldering. Classification 2 is the minimum acceptable classification recommended for SMT wave soldering.

Hybrid circuit manufacturers typically employ SN62 solder which contains some silver in the solder alloy. This solder retards the leaching of palladium-silver chip terminations. SN62 is 62% Sn, tin; 36% Pb, lead; and 2% Ag, silver. It has a melting range of 179°-183°C. Reflow of this solder is usually done at 225°-235°C. As the solder leaches silver from the termination, the melting point of the alloy increases. At 3% Ag the melting point rises about the reflow operation temperature aiding in slowing the leaching effect.

Higher temperature reflows greater than 320°C peak temperature are also not uncommon in power hybrid circuits. Sn10 (10% Sn, 88% Pb, 2% Ag) or Sn5 (5% Sn, 95% Pb) with melting points near 300°C are typical of the solders used. Even though for these high temperatures it would be expected that leaching would be increased, but due to the use of low tin content solders, terminations suitable for normal hybrid soldering are generally acceptable. Some chip types are not suited for these higher temperatures. Suitability for high temperature soldering processes should be specified in purchase specifications.

#### 4.3 CHIP MOVEMENT AND STANDING ON END - REFLOW SOLDERING

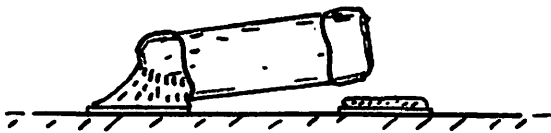
Chips for reflow soldering typically have not been glued in place. They can move out of position during the time when the solder paste loses its adhesion to the chip in the preliminary stages of soldering. Prior to reflow these chips are held in place by the dried solder paste. If the substrates or boards are reflowed while moving any jerkiness in the motion can contribute to chip movement. In some vapor phase systems, the puddling or flow of condensate may also contribute to chip movement.

Chip movement, after wetting by molten solder, is restrained by proper pad design and chip placement. Pad designs for reflow soldering is found in section 3.1. Pad sizes and the amount of solder on each should be equal. It is also important that the chip termination bands be of approximately equal size. Chips will move in molten solder to equalize the surface tension forces caused by the solder wetting the terminations. On properly designed pads, the chip will tend to align itself with the mounting pads.

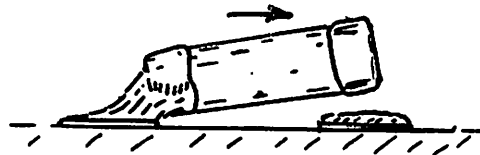
The most extreme example of the failure to wet each termination equally or at the same time is called drawbridging or tombstoning. One end of the chip is raised above the pad and fails to bond. If one termination wets before the other, that termination can lift the other end of the chip due to the surface tension on the wet termination end surface. If the solder is molten at the other termination, but has failed to wet it, a lifting force at that end can contribute to the effect

due to the tendency of that end to float. If the chip is misplaced on the pads in the direction of the chip's length axis, one end may be close to the edge or over the edge of the mounting pad. Even if equal wetting occurs, there is at that moment no opposing end fillet to hold that chip end down, particularly if the termination band widths are on the small side of the dimensional allowance. In processing where there is the tendency to drawbridge the use of chips with wider termination bands reduces the drawbridge effect. This is true where the pads are sufficiently wide enough to allow for fillets to form at the sides of the chip.

Mounting on smaller pads with minimal pad or band extension beyond the placed chip will also help reduce drawbridging. The effect is particularly notable for the smaller chip sizes such as the 0805. Limiting the fillet size by limiting the solder paste thickness is also beneficial where practical.



One End Wets Before  
The Other



Chip Misplaced, Chip End  
At Outside Edge Of  
Mounting Pad

This drawbridging is more pronounced on lighter weight, thinner chips. A length to width ratio for the chip which is less than 2 is also a contributing factor. Thicker chips will also drawbridge especially where there is a larger amount of solder paste available to form large fillets. Testing where solder pastes are applied in large amounts not typical of the production process tends to cause drawbridging on the test boards.

To avoid drawbridging, the following contributing factors should be minimized when possible.

- Poor solderability of chip terminations, including the tendencies of the termination to leach during the soldering process.
- Improper pad size and spacing. (Smaller pads in the B dimension may be beneficial.)
- Small or unequal termination band width, bottom and side surfaces.
- Improper initial chip placement.

- Vibration of assemblies during soldering.
- Unequal heating at the termination pads.
- Poor quality solder paste, oxidized.
- Large quantities or unequal quantities of solder at the ends of the chip.
- Improper soldering temperature.

The problem of chip movement and drawbridging has been reported more frequently for vapor-phase soldering. IR reflow may have less problems due to better solder wetting conditions the result of higher soldering temperature and direct activation of the flux by the IR radiation. Heating rates may also be a factor with the solder paste receiving more energy and heating faster than the chip termination.

#### 4.4 THERMAL COEFFICIENT OF EXPANSION AND BOND RELIABILITY

The mismatch in TCE between the chip and the substrate or board results in stress. Soldering typically occurs at temperatures above 200°C, but most solders used solidify at a lower temperature, approximately 180°-185°C. As the assembly cools from soldering, chips that have a TCE higher than the substrate, such ceramic substrate materials as alumina and beryllia for example, the chips shrink more than the substrate resulting in tension at the chip terminations. Weak metallization bonding or chips weak due to defects in the chip ceramic may be pulled apart by rapid cooling. This stress relaxes with time, absorbed by the solder fillet.

Just the opposite effect occurs when the chips are mounted on glass epoxy circuit boards which have a higher TCE than the chips. Chips are better able to withstand compressive forces applied at the terminations when cooling from the soldering operation. On a circuit board the plastic resin also absorbs some of the stress, especially above its glass transition temperature. Common circuit board material don't effectively apply stress to chips until the temperature falls below approximately 120°-130°C. Some high temperature circuit board materials have glass transition temperatures above the solder melting point. The mismatch between the chip capacitor and the board or substrate is more of a problem for larger chips. As chip length increases beyond 0.125" (3.2mm), more failures may be anticipated.

Repeated temperature cycling will generally cause either a mechanical failure in the chip, failure in the solder bond or failure in the mounting pad or land attachment to the substrate or board. Higher temperature solders with higher lead content are better able to withstand temperature cycling. Repeated testing often ends, therefore, in chip termination failure or breakage of the chip body. Softer solders with softening points below 200°C such as SN60 or SN62 generally will fail due to work hardening during cycling. The stress builds up on the chip as well, but the solder may fail first. Which fails first is often a function of the amount of solder in the bond and the fillet configuration. Chips which are raised above the substrate on a solder pedestal (.003" to .006") will have a better chance of survival, especially with smaller fillets.

Chips soldered to circuit boards are placed in tensile stress when reheated for additional soldering. Circuit boards also tend to warp on heating so that chip breakage is more a problem in this situation. Once soldered to the board, reheating for additional soldering is not recommended and if done should be carefully monitored.

There is significant variability in the strength of termination bonding to the chip as well as variation in the inherent strength of the ceramic dielectric. This strength tends to decline with increasing crystal grain size typically associated with increasing dielectric constant. The strength may also be reduced by defects in the chip structure such as cracks, splits or delaminations.

The TCE of barium titanate capacitors varies in the available reference material. It falls between the TCE of ceramics such as alumina and printed circuit board laminates. The lower dielectric constant Class I dielectrics have the lowest TCE's apparently in the range of 7 to 8.5 ppm per °C. Class II and III dielectrics (X7R and Z5U) are higher, perhaps as high as 12 ppm per °C.

<u>Material System</u>	<u>TCE PPM/°C</u>
FR4 Epoxy-Fiberglass Board in X-Y Plane	14-15
95% Alumina Ceramic	7-7.5
99% Alumina Ceramic	7.5-8
Porcelain on Steel	13-14
Porcelain on Invar	3-4

Note that invar foil used in plastic circuit board laminates may result in a TCE similar to that of alumina.



#### 4.5 AUTOMATED CHIP PLACEMENT

In recent years, chip placement has changed from the hand placement of chips by tweezers to the pick and place of machines rivaling the speed of leaded part insertion machines. There are many different mechanisms, some of which place many chips simultaneously, others pick and place the chips one at a time per head mechanism.

Some machines are fed by vibrating bowl feeders stocked from bulk chip packaging. These systems best handle chips which can easily be oriented end to end versus side to side. Generally, chips with a length to width ratio of 2:1 or higher are preferred. Such chips include the 1005, 1505, 1206, 1805 and 1808; all popular in hybrid design. Chips such as the 0805, 0907, 1210, 1812 and 1825 can be more difficult to orient properly, length versus width.

Other chip placement machines are fed by vibrating linear track feeders. Each vary slightly in capability and design. To avoid jamming some may require tighter dimensional control than that required for tape packaged chips. Non-standard dimensional specifications should be avoided. Characterization of chips from various manufacturers based on suitability for use in these mechanisms but within the manufacturer's specifications is not a recommended practice. The vendor may shift dimensions within their product specification based on the use of different dielectrics or even from month to month changes in process control.

Square cross-section chips, where actual thickness is close to nominal width, are also difficult to orient with the top-bottom surfaces in the proper up-down placement. The chips may be mistakenly placed with the side surfaces in an up-down orientation instead. Square cross-section chips for practical purposes may be defined as those chips where the difference between the actual chip thickness and nominal chip width is small, 0.010" (0.25mm) or less. Square cross-section chips are easy to use where this up-down orientation is not a concern such as in vibratory bowl feed mechanisms but present packaging difficulties where tape carriers are employed. As a result, chip thicknesses, despite purchase specification maximum thickness specification, are commonly 0.010" or more thinner than the nominal chip width dimension.

#### 4.5.1 8MM TAPE PACKAGING

EIA specification RS-481 covers the requirements for tape carrier and reel packaging of chip components. The most popular taping is done in 8mm wide carrier tape with sprocket holes at a 4mm pitch. Part cavities are also normally at a 4mm pitch. On 7" diameter reels similar to those used for movie film or tape recorders, up to 5000 chips may be packaged. Wider tapes are also used, typically 12mm carrier tapes. Larger reel diameters are also available which hold 10,000 chips. Capacitor chips with thicknesses which are greater than .031" (0.8mm) on 7" diameter reels are supplied with 4000 to as few as 2000 per reel (8mm tape) depending on actual chip thickness and type of carrier tape.

Cardboard carrier tapes are commonly used which have cavities punched through the tape of appropriate size for the different chip sizes. This carrier tape is from 0.8 to 1.1mm in thickness (0.031-0.043"). The chip's thickness is usually specified to be within the thickness of the tape so the chip will lie in its cavity without protruding above the carrier tape. Chips are held in the cavities by thin covering tapes adhered to the cardboard on both sides. The bottom tape is affixed before component placement and is adhered to the total available carrier tape surface. The top tape is placed a few moments after the chip is placed into the pocket. The top tape is sealed to the cardboard in continuous parallel tracks at the sides of the cavity in the direction of tape travel.

Chips must not be stuck or attached to the tapes. The top covering tape when peeled away must not pull any chips from the pockets. Similarly, turning a tape over with the top cover removed will allow all chips to fall out of the exposed pockets without sticking.

An alternative carrier is formed from an embossed or pocketed plastic or plastic coated aluminum foil carrier. The carrier tape thickness itself is typically 0.25 to 0.3mm thick (0.010-0.012"). It is formed with pockets to an overall thickness to 2mm (.079") in the 8mm wide carrier. Wider carriers may have deeper pockets. A 2mm thick overall dimension will have a pocket capable of holding a chip with a recommended maximum of 1.7mm (.067"). Because the thickness of the carrier tape must be added to both the cover tape and the pocket depth dimensions, a 7" reel will hold significantly fewer chips when compared to cardboard tapes, typically 2000 to 2500 chips versus 4000 to 5000 chips.

TAPE CARRIER TYPE

COMPARATIVE ADVANTAGES

Paper/Cardboard

- . Thinner tape allows more parts per reel.
- . Less expensive materials.
- . Acceptable to all tape fed placement mechanisms.

Embossed, Pocketed Carrier

- . Accepts wider range of chip thicknesses.
- . Available in wider sizes for larger chips.
- . Cleaner tape, no paper lint or particles.
- . Chip release is superior, also tends to feed better.
- . Does not deteriorate or absorb moisture in storage.

Cardboard or paper tape carriers were the first in use. They were designed to feed both ceramic resistor and capacitor chips of similar thickness, typically 0.6mm (.024") thickness. These carriers are also used to feed chips up to 1mm (.039") thick which doubled the capacitance value available in any given basic size at the same dielectric characteristic and voltage rating. These thickness dimensions generally are in somewhat of a conflict with the product specifications which allow for thicker chips which can not be conveniently packaged in punched cardboard carriers.

As in the section above (4.5), the requirements for proper chip orientation are applicable. There is a minimum difference between the actual thickness of the chip and its nominal width that must be observed to ensure proper chip orientation. The thickness should be a minimum of 0.25mm (.010") less than nominal width. Chips specified with maximum allowable thicknesses which are close to or the same as the nominal width such as the 0805 at .050" max. thickness and the 1206 at .060" max. thickness must be actually .040" and .050" max. thickness respectively for proper orientation and tape packaging. This thinning tends to decrease the available capacitance value range over the nominal chip specification.

8mm Tape Package

<u>CHIP SIZE</u>	<u>CHIP MAX. THK.</u>	<u>PREFERRED CARRIER TYPE</u>
0805	To 1mm (.039") To 1.3mm (.051")	Cardboard or Plastic Embossed Orientation Problem, not Recommended
1206	To 1mm (.039") To 1.3mm (.051") To 1.6mm (.063")	Cardboard or Plastic Embossed Plastic Embossed Orientation Problem, not Recommended
1210	To 1mm (.039") To 1.7mm (.067")	Cardboard or Plastic Embossed Plastic Embossed

12mm Tape Packaging

1812	To 2mm (.080")	Plastic Embossed
1825	To 2mm (.080")	Plastic Embossed

In general, the chip thickness should conform to the pocket or cavity depth. Chips which are .024" (0.6mm) in actual thickness should not be packaged in pockets .039" (1mm) to .067" (1.7mm) deep. The actual chip thickness required to avoid problems in packaging and chip removal from the tape should be no more than .016" (0.4mm) thinner than nominal cavity depth, .010" (0.25mm) would actually be preferred. This requires that for chip sizes such as the 1206 where three or more basic thickness (for example: .024", .031", and .0375") are employed in the manufacture, two or three different tape carrier thickness may be employed in tape packaging. This affects the capability of packaging the same number of parts per reel for the given chip size. Capability would depend on the value, rating and performance characteristic requirement and may vary from one manufacturer to another.

## 5.0 ATTACHMENT MATERIALS

### 5.1 SOLDER, ROSIN AND SOLDER PASTES

Soldering of chip capacitors to a substrate or circuit board is the dominant mode of chip interconnection and mounting. The solder bond or fillet not only firmly affixes the chip to the substrate, but also serves as the electrical connection. Silver-epoxy bonding is increasing in popularity for hybrid circuit assembly but is not treated in this document.

Soldering and solder materials are subjects to be treated in depth requiring in general a high level of expertise in any electronic assembly operation. The following material is an overview intended for introduction to this critical area of electronics manufacture.

#### 5.1.1 SOLDER

Solders used for electronic assembly are metal alloys which melt at sufficiently low temperatures to join the metals or metallizations of the chip and substrate/board together forming a reliable electrical connection and mechanical bond. Alloys consisting mainly of tin (Sn) and lead (Pb) are the most common. These alloys may contain smaller amounts of either silver, indium, cadmium, bismuth or antimony for special application requirements such as lowered melting points or greater fatigue resistance.

Indium and bismuth alloys with tin and lead are available for special purpose applications. In these alloys metals other than tin or lead are major constituents.

Pure metals melt at one temperature, typically unique for each metal. Alloys of two or more metals melt at a temperature lower than one of the metals, or all of the metals in the alloy. This temperature at which melting begins is called the solidus temperature. Melting is completed with increasing temperature at a temperature called the liquidus temperature. Between these temperatures, the alloy is partially molten. In this temperature span the alloy is referred to as being in its plastic range. For many alloys there is a relative percentage for each metal where the solidus and liquidus temperatures are the same, the alloy melting in a manner similar to a bare metal with no plastic range. These alloy compositions are called eutectic.

COMMON SOLDER COMPOSITIONS - APPROXIMATE MELTING RANGES

<u>Tin-Lead Solders</u>	<u>% Tin Sn</u>	<u>% Lead Pb</u>	<u>Solidus Turns Plastic</u>	<u>Liquidus Turns Molten</u>
	0	100	--	327°C
SN5	5	95	270°C	312°
	10	90	224°	302°
	20	80	183°	280°
	30	70	183°	257°
	40	60	183°	238°
SN50	50	50	183°	212°
SN60	60	40	183°	188°
SN63 Eutectic	63	37	183°	183°
	70	30	183°	186°
	80	20	183°	199°
	90	10	183°	213°
	100	0	--	232°

<u>Tin- Lead-Silver</u>	<u>% Tin Sn</u>	<u>% Lead Pb</u>	<u>% Silver Ag</u>		
Eutectic	1	97.5	1.5	309°	
	5	92.5	2.5	280°	
	10	88	2	268°	302°
	27	70	3	179°	312°
	40	57	3	179°	289°
	50	47	3	179°	260°
	61.5	35.5	3	179°	248°
Eutectic	62.5	36.1	1.4	179°	179°
SN62	62	36	2.0	179°	189°
Eutectic	96.5	--	3.5	--	221°
	95	--	5	221°	245°
	--	95	5	305°	365°
	--	97.5	2.5	305°	350°

<u>Tin- Lead-Bismuth</u>	<u>% Tin Sn</u>	<u>% Lead Pb</u>	<u>% Bismuth Bi</u>		
	43	43	14	144°	163°
	42	--	58	139°	

<u>Tin-Antimony</u>	<u>% Tin Sn</u>	<u>% Antimony Sb</u>		
	95	5	232°	240°

The most common solders are the tin-lead alloys of 50%/50%, 60%/40% and 63%/37%. Tin content (Sn), its percentage of the alloy by weight, is commonly used to name the alloy. For example, solder alloy SN60 is tin 60% by weight. Another common alloy particularly used in hybrid assembly is SN62 which has 2% by weight of silver (Ag). See table above.

### 5.1.2 SOLDERING FLUX

Solder alloys will properly wet or flow onto clean metal or metal alloy finishes or metallizations. The role of a flux is to clean these surfaces at the time and temperature of soldering. The flux must not only remove oxides, but also prevent re-oxidation of the surface before the solder can coat the metal. The flux moves ahead of the molten solder cleaning and activating the metal surfaces for the molten solder. The flux flows away from the resulting solder joint or fillet coating adjacent areas and the solder itself. In general, this flux must be removed after soldering. Cleaning is most easily accomplished if it immediately follows the soldering operation and if the flux was not overheated beyond its recommended maximum temperature or temperature-time exposure.

Electronic grade flux materials are based on rosin or similar synthetic resins. Rosin flux is designated as Type R. This type of flux is the mildest in action and is suitable only for soldering clean, oxide-free metal surfaces.

More common are fluxes which contain rosin combined with water soluble salts called activating agents. These fluxes activated by these salts are suitable to remove slight oxidation. These fluxes are designated RMA types, Rosin Mildly Activated. These fluxes, R and RMA, are employed in chip assembly operations.

For components with wire leads or metal pins which are wave soldered to circuit boards, the most common flux is type RA, Rosin Activated. These fluxes contain more or stronger activating salts. They promote soldering of more marginally solderable finishes typical of aged components or boards with plated solder finishes. Type RA flux is usually considered to be noncorrosive. Type RA fluxes are less commonly used for SMT board soldering.

Type R and RMA fluxes are not always cleaned from substrate or board assemblies when the circuit operation generates temperatures at the board which are less than the rosin melting temperature, typically about 70°C. The rosin itself is a relatively good insulator and keeps the salts encapsulated away from moisture. Some manufacturers may even leave RA flux residues on the boards, not a generally recommended practice.

Thorough cleaning is highly recommended for chip assemblies. Flux may be removed by cleaning solvents and even water-based cleaners. The manufacturers' recommendations for the use and cleaning should be carefully evaluated and followed. What is acceptable for cleaning one flux may not be suitable for another, especially one from a different manufacturer.

Flux is commonly purchased and used in liquid form. Flux pastes are also available. In the surface mounting of chips, where the chips are not glued in place or where solder paste is not used, sufficient flux may be applied and used to attach chip components to the board prior to soldering. This bond is lost, however, at the rosin melting temperature significantly below reflow soldering temperatures. The solder in this case is supplied by the reflowing of solder coatings on the pad and/or chip.

For chip capacitors, the resistivity of the flux remaining on the board or substrate, particularly if trapped beneath the chip can be significantly lower than the insulation resistance specification for the capacitor. Trapped salts in the rosin have been implicated in failure of the capacitor chips. These salts may promote metal migration between the chip terminations or between the board-substrate mounting pads. The salts have also been implicated in the internal failure mode of capacitors operating at low voltages where they can penetrate into the capacitor with moisture and cause shorts. A clearance of 5 mils (1.25mm) is the minimum where proper cleaning beneath the chip can be expected.

### 5.1.3 SOLDER PASTES

Long familiar to the hybrid circuit manufacturer, solder pastes or solder creams are also becoming more common in the production of printed circuit boards using solder reflow techniques such as IR oven and vapor phase condensation heating. Solder pastes are a mixture of materials required for reflow soldering operations. Included are solder in the form of metal powder, the flux, organic materials acting as a vehicle and suspension medium for other ingredients as well as other additives typically proprietary to the manufacturer. The solder powder may consist of particles of irregular shape and size or may be of spherical shapes confined to certain diameters.



The fluxes are primarily solvent soluble. R, RMA and RA types are all available. The main ingredients other than the solvent vehicle are the rosin (or synthetic resins) which constitute the solids, an activator, and an additive to control viscosity. This additive is not always employed, but as a thickening agent, it helps control the rheological properties for screen or stencil printing.

In the past, deposited solder pastes were reflowed within a few hours. Today some manufacturers refrigerate and store screened on solder pastes for days. This practice must be monitored to watch for the tendency of the paste to form solder balls when later dried and reflowed. Solderability may also be affected.

Generally, drying of the paste should be accomplished within a few hours of application unless the board or substrate is reflowed within this time. Drying is done after the chips and other surface-mounted components are placed. The drying process is typically done by slowly heating to 80°C to 90°C for a period of from 5 to 15 minutes. The time to dry depends on the amount and kind of solvent which are present. Drying brings the rosin or resins to the surface holding the chip component in place. The rosin also forms a moisture barrier to protect the metals and activators covered by the paste. Solvents should be completely volatilized to reduce the tendency for splattering during the reflow operation, particularly where high rates of heating are employed. Splatters are another source of solder balls - solder which lies on the substrate outside of the pad deposition area which may or may not be removed during post-soldering cleaning.

The actual solder alloy content of the paste is normally specified by its percentage of the original wet paste's weight. A paste which is 88% to 90% solder by weight is approximately 50% solder in volume. At 80% by weight, the solder volume content is only approximately 33%. Obviously, the high content by volume pastes will provide larger fillets. These pastes also tend to slump less in drying and reflow. However, these pastes may be more difficult to screen print in a high volume production environment making it difficult to have accurate screening on small pads. Tradeoffs in percent content, processability, print height and final fillet size are made.

RMA pastes are most often used since they can best handle pastes where the solder content has become oxidized in the screening or drying process or in storage before reflow. RMA pastes also may compensate for less than ideal chip or substrate metallizations. These pastes also leave nonconductive residue after reflow if not overheated. Always know the characteristics of the paste in use. Adequate information is generally available from the manufacturer.

The solder pastes must often be tailored to the users' requirements. The amount required and the method of application are the first formulation consideration. The drying and reflow parameters are equally important. The ability to easily and effectively clean soldering residues is another parameter in paste selection. To obtain the proper solder fillets with the least defects such as solder balling and bridging and at the same time have a repeatable and economical process, is the goal.

## 6.0 CHIP PLACEMENT AND PRESOLDERING ATTACHMENT

The bulk of surface mounted components are placed on boards or substrates by automated mechanisms or production robots. There are many types of automated systems in use. Of the basic mechanisms, the most popular are pick and place heads which take one chip at a time from the feed mechanism or leading position and place it on the substrate. Multiple heads per machine or in-line placement stations are common. The pick up is either direct from the chip package, typically a tape carrier, or from a feeder mechanism pushing chips down a track from a bulk fed chip reservoir. Stick and magazine fed feeders are also available, but generally used in mass placement heads where several chips at a time are transferred from the pick-up station to the substrate. Larger, irregularly shaped, or polarized components, however, may be fed directly from sticks or magazines to pick and place feeders.

### 6.1 CHIP PLACEMENT - PICK AND PLACE HEADS

Many chip pick and place handling heads operate by a vacuum probe attachment to the chip. Some of these probes are supplemented by jaws which straighten up or align the part, centering it properly on the probe as well as holding it during transport and board placement.

The use of automated pick and place heads imposes its own requirements on the shape and dimensions of some aspects of the chip. Some mechanisms are designed to feed parts within a specified range of thickness which may not be the same as a typical chip product specification, particularly true for larger chips. Thicker chips may require the use of embossed plastic type of a carrier tape. For some chip placement equipment, special feeder mechanisms are required to handle this type of tape, especially the thicker versions. See section 4.5.1.

The surface contour of the chip can become important. The top of the chip, which is exposed for pickup, may not have sufficient flat clear area which is optimum for vacuum probe pickup and transport. Chips with thicker termination metallization may create a pickup problem. Chips with solder coatings are perhaps the worst problem. A 0805 chip has a typical minimum distance between opposite terminations of 0.020" (0.5mm), with a nominal distance of 0.040" (1mm). Probes, the outside diameter of the contacting tube, generally have dimensions from .040" (1mm) to .063" (1.6mm). Smaller probes are available for special pickup problems. The chip and probe and pickup are not precisely aligned. There is a tolerance on the probe position as well as the tape carrier pocket position and the centering of the chip in the pocket.

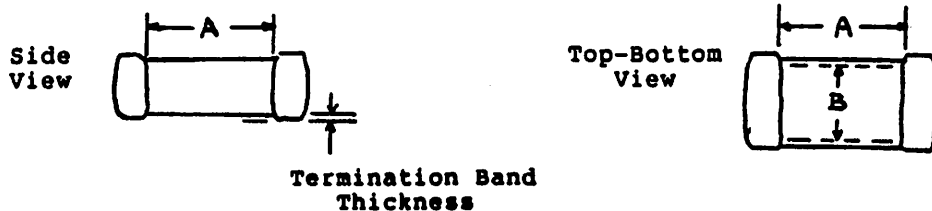
It is obvious that for the smaller chips, the probe will land partially on one of the terminations of the chip, creating a potential vacuum sealing problem. The chip may move after pickup or even fall off during rapid acceleration.

At placement the chip may be lowered to the board based on programmed chip height information which may vary for the same part number from different purchased chip sources. This is a potential problem as insertion force is required to either properly place the chip into the glue or into the solder paste in the case of reflow soldering. Placement to a specific pressure on the board is a probable advantage.

The machine in use and its characteristics must be thoroughly analyzed by the user to prevent placement problems. This is particularly important where multiple chip sources or changing chip sources are a certainty.

FLAT CLEAR CHIP SURFACE AREA  
TOP & BOTTOM SURFACES  
AREA BETWEEN TERMINATIONS

- Assumes Chips with End Band Terminations.
- Industry Specification Typical Termination Req'm'ts
- 8mm Tapeable Chips Only



Chip Size	Nominal	'A'		'B'	
		Minimum	Typ.	Chip Width	
0805	.040" (1.0mm)	.020" (.05mm)		.050" (1.25mm) Nom.	.035" (0.9) Min. Flat
1206	.085 (2.15)	.065 (1.65)		.063" (1.6) Nom.	.050" (1.25) Min. Flat
1210	.085 (2.15)	.060 (1.5)		.100" (2.55) Nom.	.085" (2.15) Min. Flat

APPROXIMATE TERMINATION METALLIZATION THICKNESS

	Mils	Microns
- Silver Alloy (Pd-Ag)	1/2 to 1 1/2	13-40
- Barrier Layer - Solderable	1 to 3	25-75
- Solder Coated	2 to 5	50-125

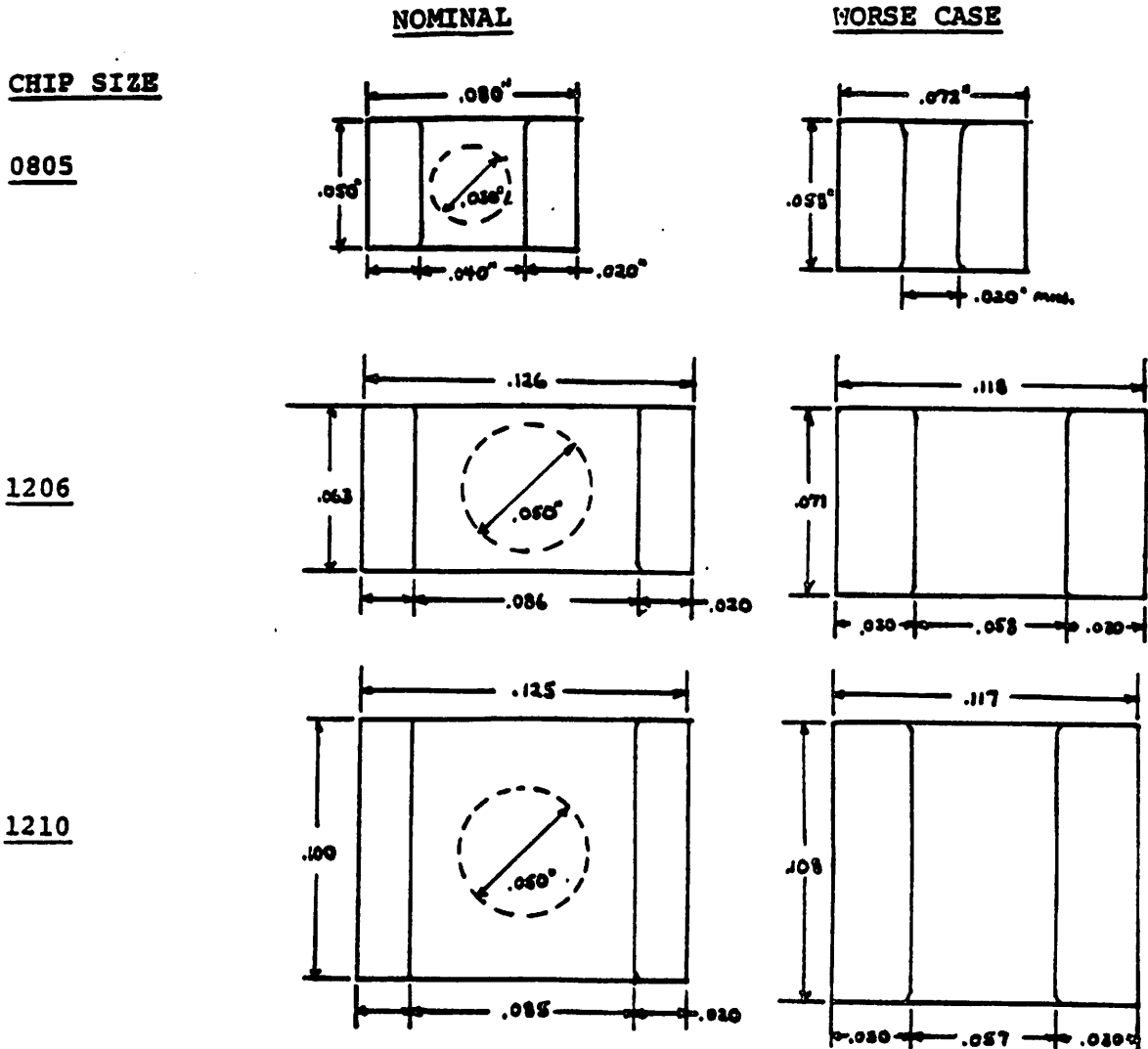
## 6.2 GLUING, PRE-SOLDERING CHIP ATTACHMENT

Chips mounted on the bottom or solder side of a circuit board with leaded components mounted on the top side must be glued to the board prior to wave or flow soldering. Commonly, these chips are placed and glued prior to leaded component insertion. Chips are also placed after leaded devices are inserted, cut and clinched, although this requires different glue deposition technique or even applying the glue directly on the chip prior to placement.

Glue is commonly placed by screen printing techniques to the bottom of the board before leaded component insertion. The chips are placed and the glue cured. In other cases the glue may be placed by glue dispensing heads just prior to chip placement. In this case the glue and chips can be placed between the clinched leads of components mounted on the other side of the board. Sometimes glue may be placed by transfer from many daubers or pins in a predetermined array or pattern. The array is first dipped into glue then applied to the board leaving behind the required pattern of glue dots with the required amount of glue.

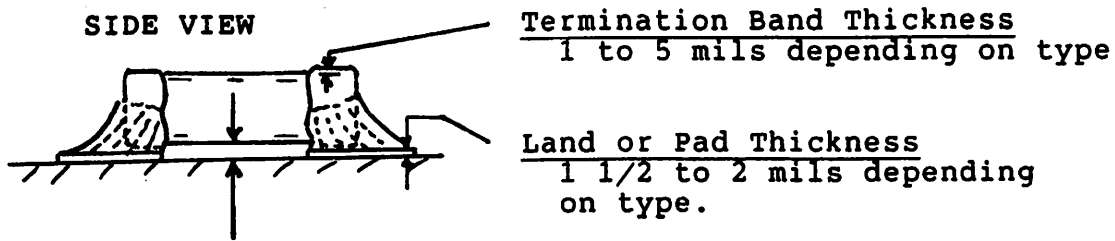
Where rough handling may be encountered, the glue bond strength between the chip and board should be determined. Leaded component insertion after the chips are glued can cause the chips to break loose. On some boards the glue may be deposited on the bare laminate, on others on a solder mask. The solder masks may be either of the screen printed or dry film type. The strength of the glue bond to the board has been found inadequate in some applications. Especially take care to evaluate the solder mask adhesion itself at preheat and soldering temperatures. Many will release the chip when heated.

In some placement machines the glue is deposited on the chip prior to its placement on the board.



The chips in the above figure compare the chip size and the clear area available between terminations to the relative size of a single glue dot. Larger diameter glue dots may be suitable for the 1206 & 1210 depending on the thickness of the glue dot and the clearance between the board and chip.

The amount of glue required and its height will vary among the different size chip components. Some mechanisms can respond to varying requirements by depositing more glue, others by placing more glue dots or bars at a specific site. The amount required is determined by the nominal mounted clearance between the chip and the substrate between the terminations and pads and by the "squish" pattern desired. Some glue must be visible around the chip for some applications such as UV curing. In this case the clearance and the width of the chip also became important considerations. The "squish" pattern should not run onto the termination or pad metal, particularly beyond the ends of the placed chip.



Termination Band Thickness  
1 to 5 mils depending on type

Land or Pad Thickness  
1 1/2 to 2 mils depending on type.

Clearance - Typically from 2 to 6 mils range  
(Subtract any coating thickness between bands or pads on the board.)

The use of four mil (0.1mm) thick glue deposits before slumping, obviously, is not adequate for the full range of mounting requirements. Mixing of different chips from one vendor to another can also create a problem. Chips, for example, with no termination bands will have a significantly different "squish" pattern than a chip with thicker terminations.

A glue dot which is essentially a circular spot of glue on the substrate works best for chips where the distance between the termination edges is equal to or greater than chip width. This allows a centered glue dot to have a squish pattern that reaches the edges of the chip body without spreading onto the terminations or their matching substrate pads. The widely used 1206 chip size meets this requirement and is the standard chip for gluing to the bottom of the circuit board.

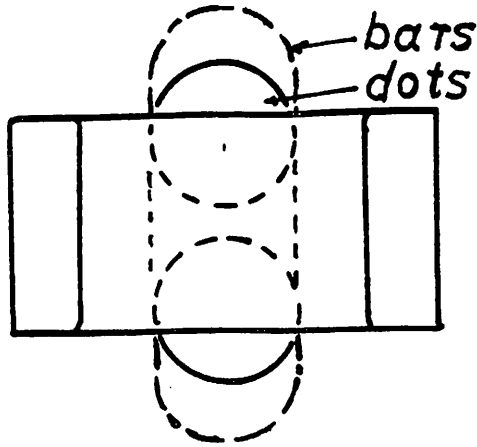
SUITABILITY FOR SINGLE GLUE DOT MOUNTING

Chip Size	Distance Between Chip Terminations		Chip Width Nom.	Adequate Area For Single Glue Dot
	Nom.	Typ. Min.		
0805	.040"	.020"	.050"	No - (.030 diameter)
1206	.085	.065	.063	Good (.050 dia.)
1210	.085	.065/.060	.100	No (.050 dia.)

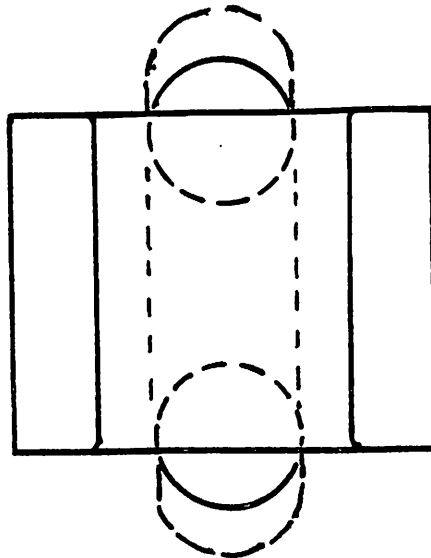
\*Assumes standard chips with termination bands.

Double glue dots placed near the opposite sides of the chip may also be used. The figure below shows the relative glue dot size and positioning. These glue dots would initially be from .040 to .050" diameter.

1206  
Size



1210  
Size





A centered glue dot of approximately .040" (1mm) to .050" (1.3mm) in diameter is adequate for 1206 mounting if a squish increases the diameter to the edges of the chip. A glue dot slightly smaller is adequate for mounting a 0805 chip size. A dot of this size can hold a 1210 chip, but no glue would be exposed at the chip sides.

Two glue dots or bars centered under the chip, but close to its edges, are also widely employed. This arrangement can provide the same adhesion to the board with less problems in contaminating the soldering pads.

## 7.0 CHIP ATTACHMENT AND CONNECTION BY SOLDERING

Soldering is, by far, the dominate mode of electronic component mounting and electrical interconnection. The following sections discuss some aspects of the various methods of soldering chip components. It is not meant to be a substitute for expertise required to implement this most critical of process steps in circuit assembly.

### 7.1 REFLOW SOLDERING, HYBRID CIRCUITS (Thick Film on Alumina Ceramic Substrates)

Reflow soldering had been the traditional and most practical method of assembling capacitor chips of various sizes and characteristics onto the metallized conductor pads fired onto ceramic substrates. Reflow soldering is the method by which terminations and mounting pads are joined by solder by the remelting of solder already present on or between these surfaces. The available solder for the bond may be only from solder coatings previously applied to the chip or the substrate. Typically, solder is provided by the application of solder paste or cream before chip placement. This solder paste is normally applied to the substrate pads by a screening operation. In rarer instances, the paste is applied to the chip prior to its placement by hand using a syringe or similar tool.

The reflow of the solder is accomplished by a gradual heating to the solder melting temperature. Continued heating to a peak approximately 30°C above the nominal melting temperature ensures good solder flow and wetting. The assembly is then gradually cooled. The total time the chip terminations are in molten solder varies from 3 to 10 seconds. Usually a low temperature solder is used with a melting point less than 200°C. The peak soldering temperature is usually in the range of 220°C to 240°C. The solder used is also typically silver bearing type to aid in limiting leaching of the silver from the terminations and mounting pads. SN62 is most commonly used.

Higher temperature solders with lowered tin content are also used in hybrid assemblies. SN5 and SN10 solder types, sometimes also containing small amounts of silver, are employed with typical peak soldering temperature at 325°C. A higher temperature solder composition commonly found, which has a low leaching characteristic, is the alloy Sn 10%, Pb 88% and Ag 2%. If high temperature soldering is to be used, the chip component manufacturers literature should be consulted for suitability. Some chip metallizations may be adversely affected by 300°C range temperatures. The assumption should not be made that components which withstand normal peak soldering temperatures of 260°C or less are suitable for higher temperature processing.

The traditional capacitor chip termination for hybrid circuits has been the palladium-silver (20% Pd) alloy. Barrier layer terminations are also available which may be used for these applications, allowing the use of either silver or non-silver bearing solders. The wetting time characteristic for reflow soldering in conduction belt ovens is not as critical as for other soldering operations.

Chips and substrates which are pretinned or solder coated have already withstood one solder reflow cycle. Mounting the chips requires a second reflow. Any rework or repair may involve yet another reflow step. Leach resistance of the metallizations may become an important factor to the manufacture of acceptable hybrid circuits.

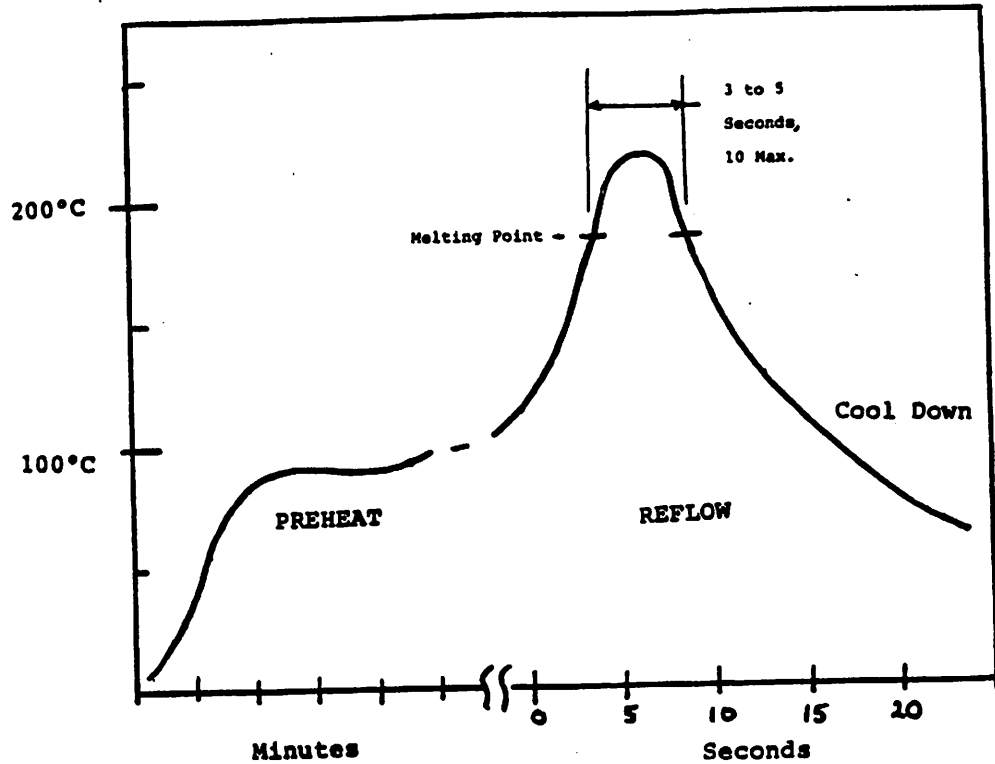
Moving belt or conveyerized soldering ovens or furnaces are most popular for reflow of hybrids. Most of the heat is supplied from beneath the belt, heating the flat bottom of the substrate lying on the belt. These systems are popular because of the controlled heating zones, adjustable belt speeds and the ability typically to observe and repair somewhat the circuits as they reflow. The systems usually take up minimal space and are comparatively economical.

Another version capable typically of greater through-put is the convection heat belt furnace. Heating is not from beneath the belt, but is accomplished in a manner similar to thick film firing furnaces from heater zones on the walls of the furnace section. Once the temperature profiles are established, this furnace system is very stable in operation. These systems can also include nitrogen-filled sections to reduce oxidation problems.

Both systems typically provide a preheating section to allow the use of non-dried solder pastes. This section also brings the chips up to a temperature approximately 100°C below peak soldering temperature to minimize thermal shock during the typically rapid rise to peak soldering temperature. The typical preheat temperature is from 80° to 125°C. The chips are at the higher temperature before entering the reflow zone.

Some production processes using predried solder paste or solder-coated terminations covered with flux omit the preheat zone. The chips are brought from ambient to soldering temperatures in less than twenty seconds, a rate of 600°C/min. This rate is impressive, but is similar to the heating rate from the preheat zone. Some systems without preheat can heat, solder, and cool down in approximately a half a minute. Preheating is recommended by most chip capacitor manufacturers.

BELT FURNACE APPROXIMATE  
TEMPERATURE PROFILE



7.2 REFLOW SOLDERING, PRINTED CIRCUIT BOARDS

Chip capacitors which are reflow soldered are typically mixed with other components, both leaded and leadless, mounted on the top side of the circuit board. The chips are typically mounted first along with other leadless or surface mounted components, then soldered. Leaded parts are then mounted and wave soldered in the normal procedure. The solder used on the top side will not be sufficiently heated to remelt and flow.

Advances in soldering technology may allow the simultaneous, or at least on the same machine, reflow of surface-mounted parts on the top of the board and wave soldering of both leaded and chips on the board bottom.

7.2.1. CONVECTIVE TUNNEL OVEN REFLOW - PCB

This reflow technique was adopted from hybrid circuit soldering. A conveyor belt transports the boards through a tunnel oven with several controlled heating zones. This gives a good control over the soldering profile. The process is reportedly very stable with repeatable results.

Thermal shock to chips is less for this process than for other reflow techniques such as IR and vapor phase. Circuit board materials will behave differently during heating. Materials that withstand the process without damage such as scorching or warping must be selected. The time for temperature excursion above the solder's melting temperature should be restricted to a maximum of 10 seconds; 3 to 5 seconds is typically long enough for good solder bonding.

### 7.2.2 IR REFLOW - PCB

Infrared radiation is a major heating source for obtaining solder reflow in production. The IR energy is provided by lamps or specially muffled, panel-type heat sources. Both the board top and bottom sides can be heated, sometimes with different temperature profiles. The IR furnaces commonly used are of the unfocused source variety with a broadened spectrum of wavelengths. This tends to protect heat sensitive parts from overheating yet at the same time improve uniformity of heating.

Heating tends to be a function of the emissivity of the materials and their inherent thermal conduction. Solder pastes absorb the IR radiation and heat quicker perhaps than the chip metallizations. The radiation reportedly directly activates the cleaning action of the flux better than other reflow techniques resulting in superior wetting activity and better solder bonds. To heat the solder paste, however, it must be exposed to the radiation on the pads beyond the chips and surfaces. If it is shadowed, the reflow action is not perhaps as good. In some IR furnace set ups, hot air actually supplies a large portion of the heat required for soldering. In these cases the shadowing is not as important. This means that some attention must be paid to pad dimensions and part placement. Other reflow techniques using smaller pads may accommodate higher density chip-mounting requirements.

IR soldering equipment using non-focused IR generally retain the chips and boards at soldering temperatures in the range of 200°C to 250°C for a few minutes. In this case, leach resistant terminations become important to soldering.

### 7.2.3 VAPOR PHASE REFLOW - PCB

Heating is accomplished by the condensation of fluorocarbon vapors. Heating rates of all exposed surfaces is very uniform and repeatable from assembly to assembly. The fluorocarbon typically used boils at standard pressure at 215°C. Higher temperature fluorocarbons are also available, specifically one that boils at 253°C. The latest vapor phase reflow equipment are in-line systems using a conveyer belt. Batch systems are also in use.

Soldering results are highly reproducible. The immersion time required for reflow varies from a minimum of ten seconds to approximately 2 minutes or longer. The time typically depends on the mass of the largest devices to be soldered. If a higher temperature fluorocarbon is used, the heating time must be reduced significantly.

Due to the lower soldering temperature, more attention must be paid to the solder chosen. SN63 eutectic with a melting point of 183°C is suitable. Others use standard SN60 solder with a nominal melting point of 188°C. Lower temperature solder alloys are also used in an effort to improve wetting characteristics. SN62 2% silver bearing solder has a nominal melting point of 189°C, but an enrichment of the silver percentage due to leaching rapidly raises the melting temperature. At 3% silver content, the melting temperature rises to over 240°C, well above the reflow temperature. SN62 solder is not recommended for vapor phase reflow at 215°C.

Due to solder wetting problems and perhaps due to the presence of the condensate on the board, more problems with small chips draw-bridging or the movement off one of the mounting pads have been reported. Care in process implementation, design and selection of components with high solderability are reported to overcome these problems.

Vapor phase soldering has the early reputation as the best approach for the mounting of IC chip carriers on boards using small, high density mounting pads and interconnections. IR and other techniques may, however, be more productive for simpler, less sophisticated surface mount technology boards particularly when produced in large production runs.

### 7.3 FLOW OR WAVE SOLDERING - PCB

Flow soldering differs from reflow soldering in several key ways. The heat or temperature required at the termination to effect soldering and the amount of solder required are provided by a momentary immersion in molten solder. The solder is typically at a temperature in the range of 240°C to 260°C. This immersion in wave soldering is accomplished by moving the boards on a conveyor so that the board bottom passes through a standing wave of molten solder. The time in the wave is only for a few seconds, as the boards are moving at a rate of one to two inches per second. A fluxing and preheat zone is included before reaching the solder wave.

Chips are mounted on the bottom of the board, held in place by glue between their terminations and the board surface. Wave soldering allows the simultaneous soldering of leaded devices and surface mounted devices on the board bottom. The solder fillet produced typically shows wetting of the top and sides of the termination band as well as the end surface of the chip. Solder will also flow under the chip, but may be interfered with by glue on the mounting pads or lands. The primary fillet is the area visible at the chip ends.

Because of problems in wetting the chip terminations in standard wave soldering lines, new techniques have been developed. Dual solder waves and special solder waves have been employed to fully immerse the termination in hot solder for the length of time required for a good fillet; this time is typically one second minimum. To aid in this soldering, chips are commonly specified with solder finished terminations, typically tin or tin-lead plated over the primary silver metallization. A barrier layer may also be incorporated to minimize leaching and damage to the chip termination. Some of the newer wave soldering lines expose the components to extended time periods above the solder melting point. Instead of a few seconds, the total exposure time can be 10 seconds or more. For this reason some manufacturers choose to run at lower temperatures, 235°C.

The orientation of chips, their spacing, and relative positioning to other chip components on the board bottom are also significant factors in soldering. Because the parts are flowing through the solder, a shadowing or masking affect may occur. Chip terminations trailing through the solder with the chip oriented along its length axis in the direction of flow, will tend to have smaller fillets and more difficulty in forming acceptable bonds.

Similar chips shadowed by close and larger components will tend to be masked out of the solder flow producing similar effects. Care should be taken in component layout to minimize these problems. Newer soldering lines using dual-waves and other techniques have made shadowing much less of a problem.

#### 7.4 CLEANING AFTER SOLDERING

The residues resulting from soldering typically require thorough cleaning. The residues consist primarily of the flux ingredients initially present prior to soldering as well as new compounds formed from heating including carbon or carbonaceous materials. In some cases, depending on operating temperature and environment for the finished assembly, these residues represent ionic contamination which can support metal and metal salt migration. These can lead to insulation failures on the board and chip surfaces. They can penetrate the chip itself, in some cases causing shorts. Reliability concerns for long circuit functional life typically dictate great care for thorough board and substrate cleaning.

As in the case of soldering, cleaning is not a subject which can be adequately covered in the few following paragraphs. The following information is only meant to be an overview. Expertise must be brought to bear in the assembly process in this as in other areas to ensure defect free quality manufacturing.

Cleaning is accomplished by either solvents, typically alcohols or glycols combined with fluorocarbons or by water and detergents. Solvents are used in commercial vapor defluxing equipment. Typically, in either cleaning method, several steps are taken in the cleaning process to ensure removal of residues and ionic contamination, particularly chlorides. In some cleaning processes, both solvent and water based cleaning method are employed. Ultrasonics are also employed to aid in cleaning.

An important consideration for cleaning assemblies with chips is the ability to get under the chip to attack flux residues and rinse out the materials. Solvent-based systems possibly are better at penetrating these spaces, particularly aided by ultrasonic agitation.

A method of measuring the effectiveness of the cleaning operation is highly recommended. Extraction methods are perhaps best at yielding an indication of cleaning under surface mounted devices. Other methods which test the exposed surface of the board or substrate may not be reliable in determining the cleanliness of the surfaces under the chips.



